Single Event Upset tests of Commercial FPGA for Space Application

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Saab Ericsson Space Group

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Saab Ericsson Space Products

Command and Data Handling Systems

for more than 60 satellites

Guidance and Control Computers

for more than 130 Ariane launchers

Payload Processing and Control

for Inmarsat, Galileosat, Envisat, Metop...

Mass Memories

for Rosetta, Leostar..

GPS Instruments

for Metop/GRAS, NPOESS/GPSOS

Presentation

- Space vs LHC
- SEU Basic Mechanism
- FPGA Technologies
- Single Event Upsets ; Heavy Ions
- Single Event Upsets ; Protons
- Single Event Transients
- Conclusions

Space vs LHC

	Space Missions	LHC Experiments
• Mission Time	*10-15 years*	*10 years*
• Service	*Not Possible*	*Impractical*
• Electronics Reliability	*High*	*High*
• Total Dose Requirements	*10 -100 krad*	*1 krad - 10 Mrad*
• Single Event Upsets	*IC's SEU characterised* *No Critical SEU Accepted* *Risk Mitigation*	*?*
• Costs for Electronics	*FPGA 200-300$ / kGate*	*"Less"*

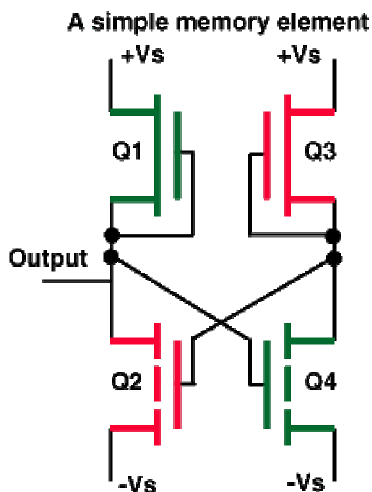
COTS

- Consumer Electronics
  - Produced in High Volumes
  - Product under Continuous Development
    - Short live time
  - Product under Continuous Yield Optimization
    - Small changes to mask-set /Shinking
- Electronics Produced for the Space/Mil Market
  - Controlled & Screened to a SMD
  - High Degree of Tracebility , reliability
  - Low Volume/High Cost

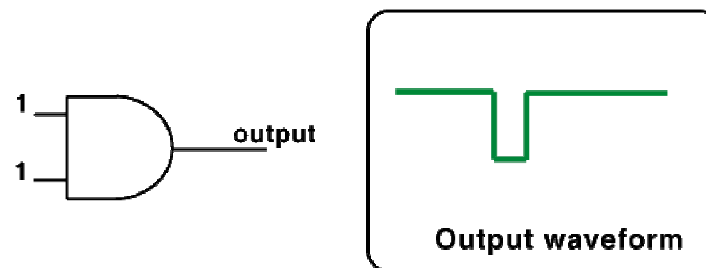
Single Event Effects

Soft Error

Single Event Upset



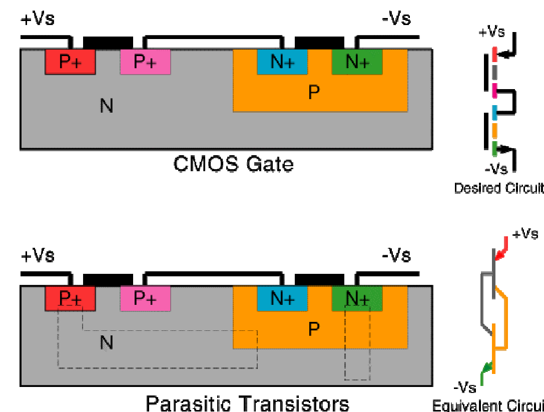
Single Event Transients



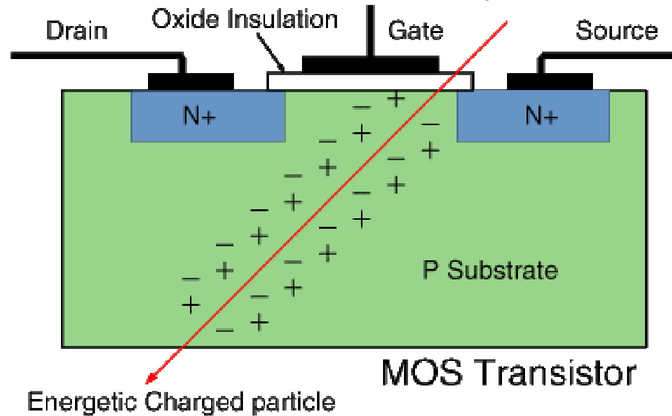
Hard Error

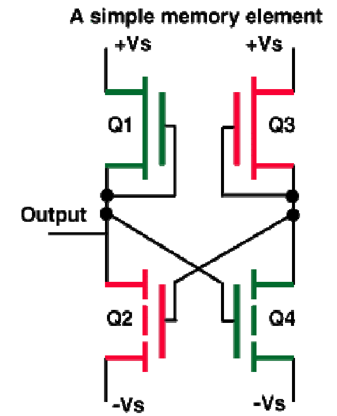
Single Event Latch-up (LU)

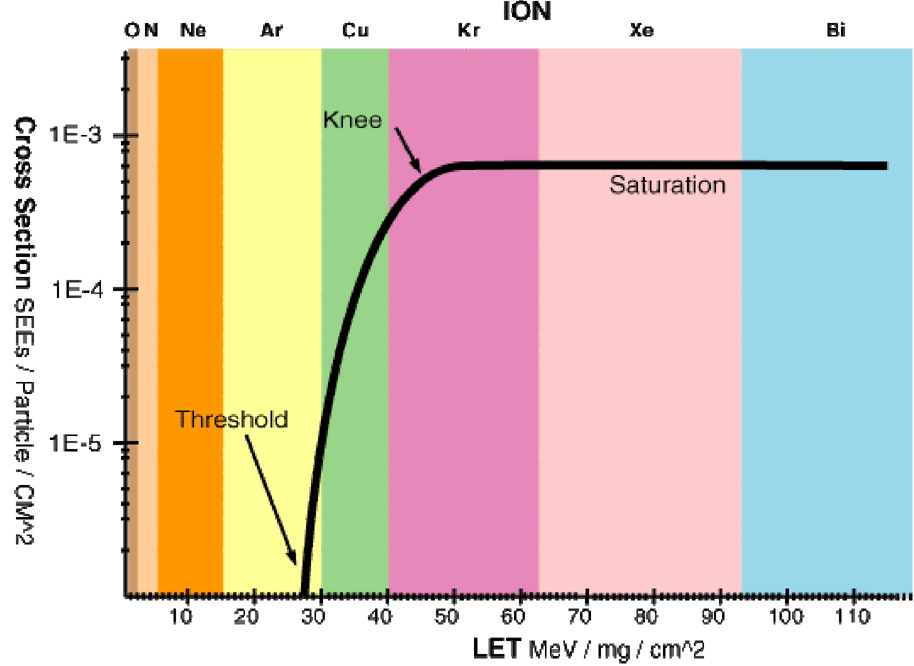
Charge Particle activated Parasitic Transistor

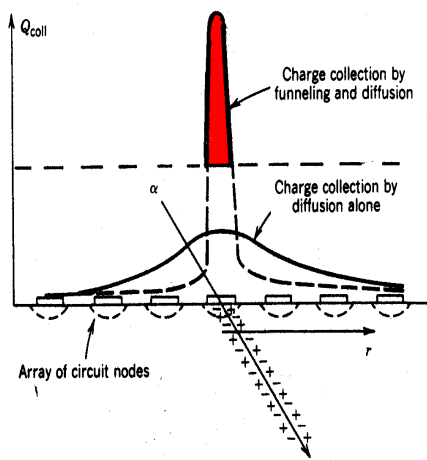


Single Event Upsets









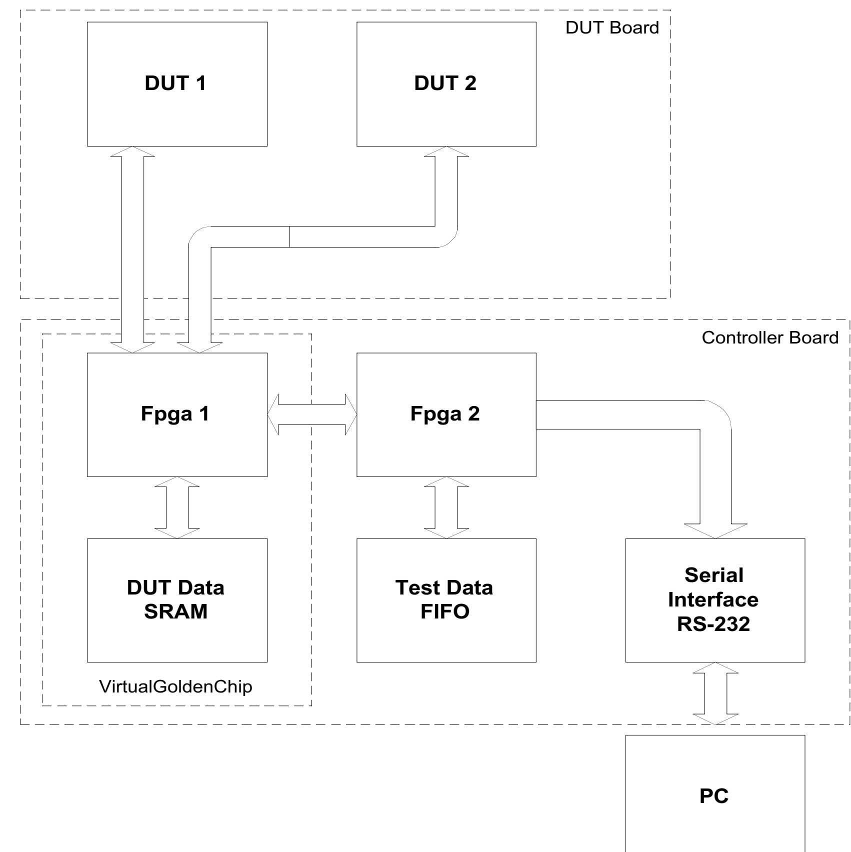
Single Event Upsets

SEU Vulnerability Dependent on

- Manufacturer Technology / Process
- Design of Bi-Stable Element, (4T-, 6T-, 10-21T-cell)
- Design / Layout of Function into IC (Size)
- Lower Bias Condition - Worse for SEU
- Smaller Feature Size - Worse for SEU

SEU Test Set-Up

- Interpreting SEU Results - Non Trivial
- Strive for Simplicity in SEU Tests



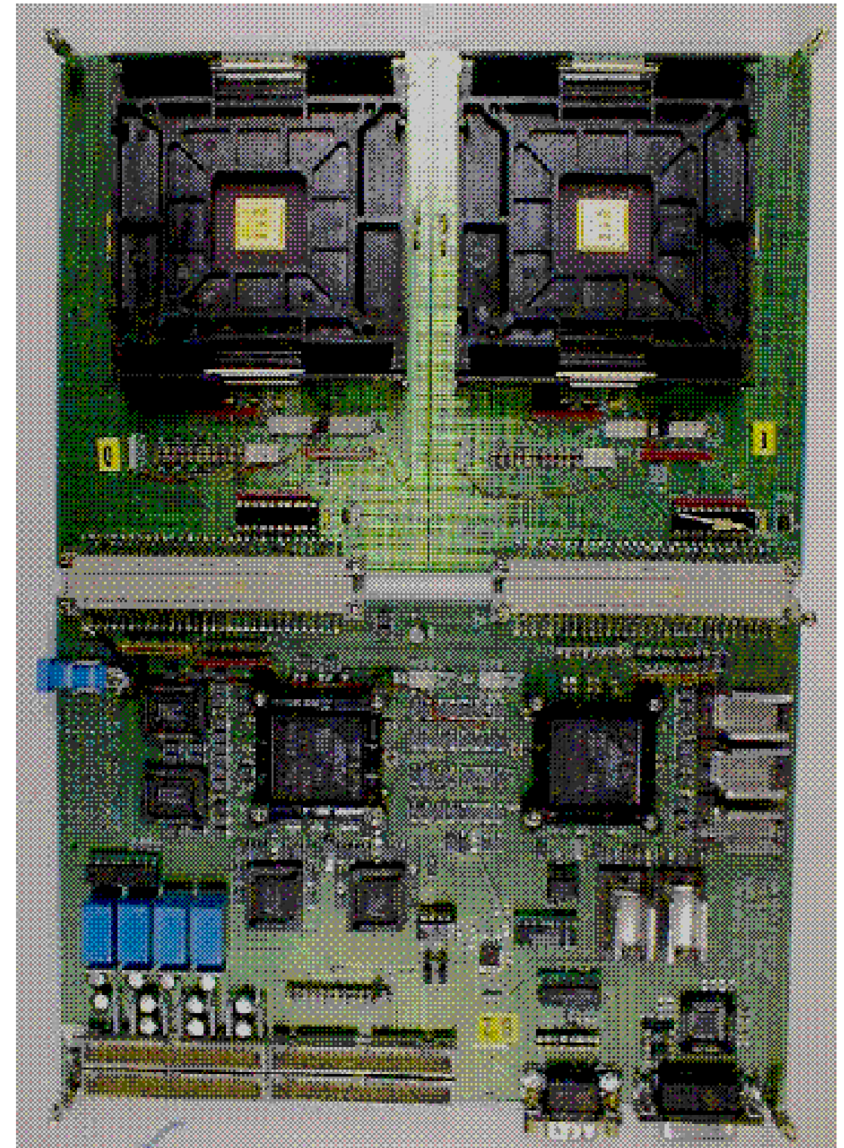
- Golden Chip Test Method
  - Shift Registers, 64 bits
  - Test Pattern, 1 0 1 0 1 0….
  - Static

    Load data, 5 MHz
    Pause Pre-set time (1s)
    Read out/ Compare, load data
  - Dynamic

    Load/ Read-out Compare, 5 MHz

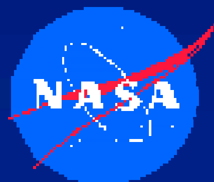
SEU Test Set-Up

Test Boards for Accelerator Tests

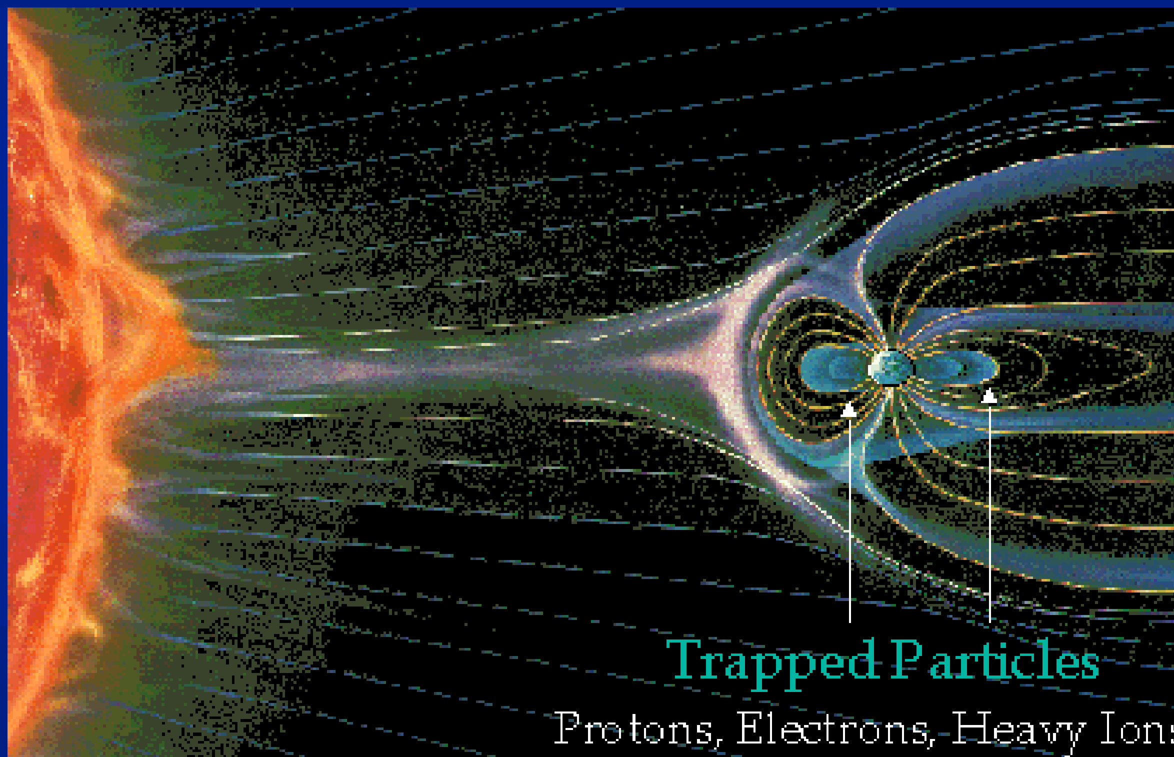


Heavy Ions
- Vacuum Chamber
- Delidded
  - Range in Si 20-40µ
- Equipment close to DUT

Protons
- In Air well shielded
- Equipment far Away

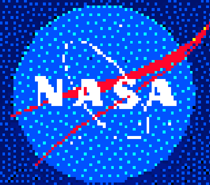


Trapped Radiation



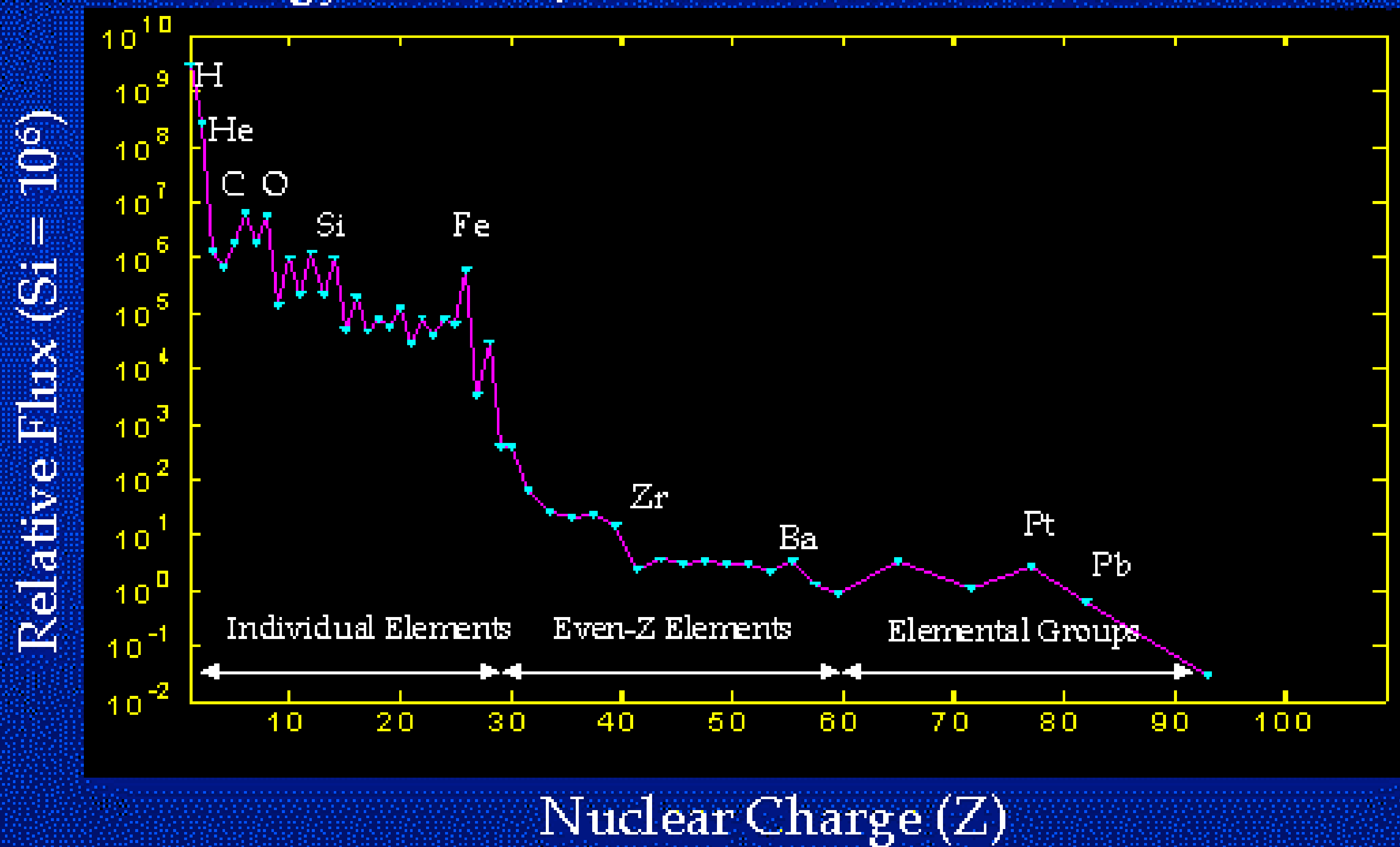
Nikkei Science, Inc. of Japan, by K. Endo

J. Barth/IEEE-NSREC Short Course 1997



GCRs: Nuclear Composition

Energy = 2 GeV/n, Normalized to Silicon = 10^6



J. Barth/IEEE-NSREC Short Course 1997

Antifuse Based FPGA

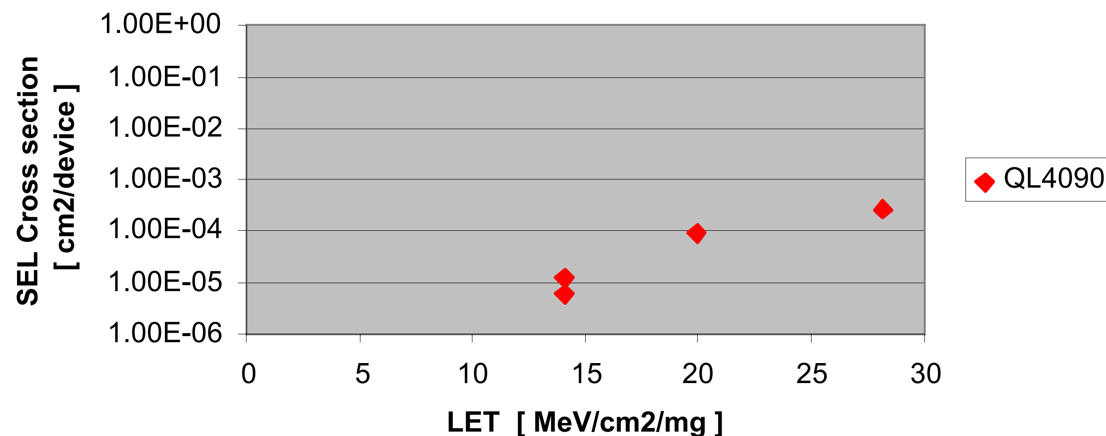
- Concern
  - SEU in User logic (FF)
  - Corruption of Fuses
  - LU

- ACTEL (MEC Only)
  - A14100A, 0.8µ ONO 10 kgates, #FF (S-697, C-680)
  - 54SX16 /(32), 0.6µ Metal-to-Metal, 16 kgates, #FF (R-528, C-928)
  - 54SX32-A / -S, 0.25µ Metal-to-Metal, 32 kgates, #FF (R-1080, C-1800)

- QuickLogic
  - QL4090, 0.35µ,
  - SEL

- Aeroflex UTMC

  UT4090, 0.35µ
  90 kPLD gates, hard FF
  (Will be tested this autumn)



SRAM Based FPGA

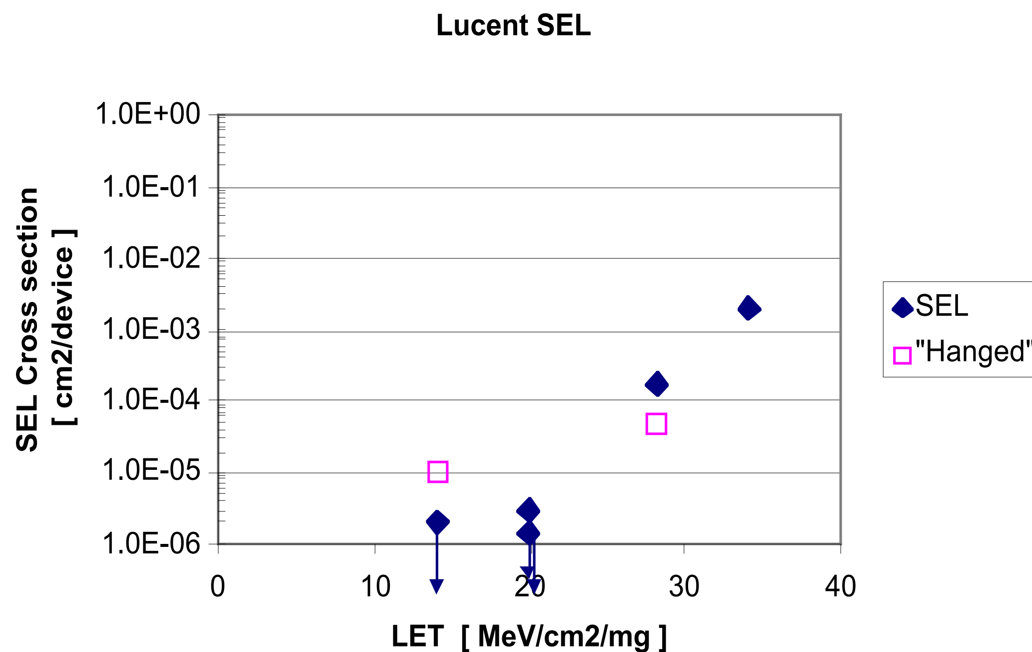
•Concern

- SEU in User logic
- SEU in Configuration logic
- SEU in Architectural logic
- LU

- Xilinx, 2.5Volt
  - Virtex QXPR300 0.22µ
  - 300 kgates, #FF (6144)
- Lucent, 5Volt
  - OR2C06A- T 144 0.35µ
  - Usable PLD gates=15700
  - Registers/LUT=576
- Atmel, (3.3Volt)

  AT40k, 0.35µ, Rad Hard FF

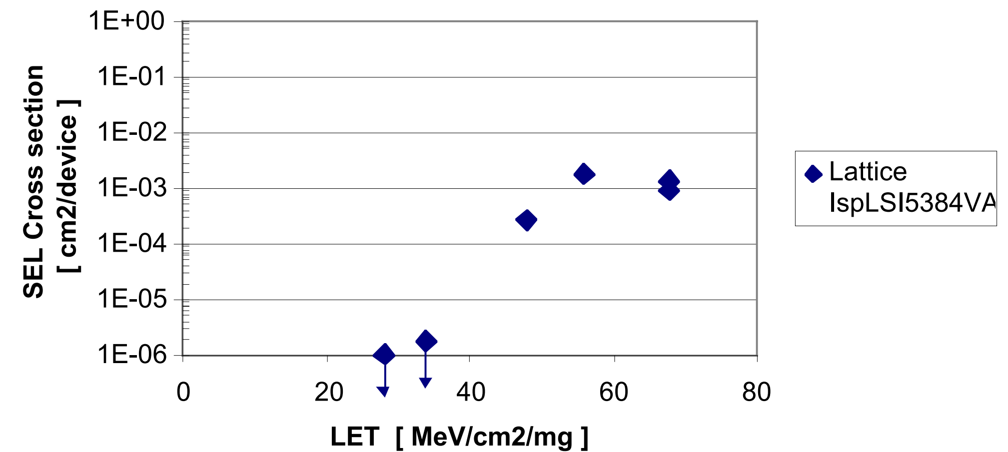
  (vill be tested beginning next year)



Non Volatile FPGA

- Concern
  - SEU in User logic
  - SEU in Architectural logic
  - LU

- Lattice, 3.3Volt
  - ispLSI5000V, μ
  - 18 kgates, #Registers (384)
  - Re-programmable on board



- ProASIC 500k (Actel)

  Flash/CMOS 0.25μ

  System gates - up to 500k

  "SEL was detected immediately upon opening of the shutter" (R. Katz, GSFC)

SEU Results
Actel A14100A

- 0.8µ Matsushita (MEC)
- "10000 Gates", ONO
- Logical modules 1153,
  - S-cells 697
  - C-cells 680,
- User I/O's 228

Asymmetric Flip-Flop

1→ 0 more sensitive than 0 → 1

Proton Sensitive

A14100A Vcc=3.3V & 5V

3.3V

Limit Proton SEU

Cross Section (cm2/bit): 1.0E-04, 1.0E-05, 1.0E-06, 1.0E-07, 1.0E-08, 1.0E-09

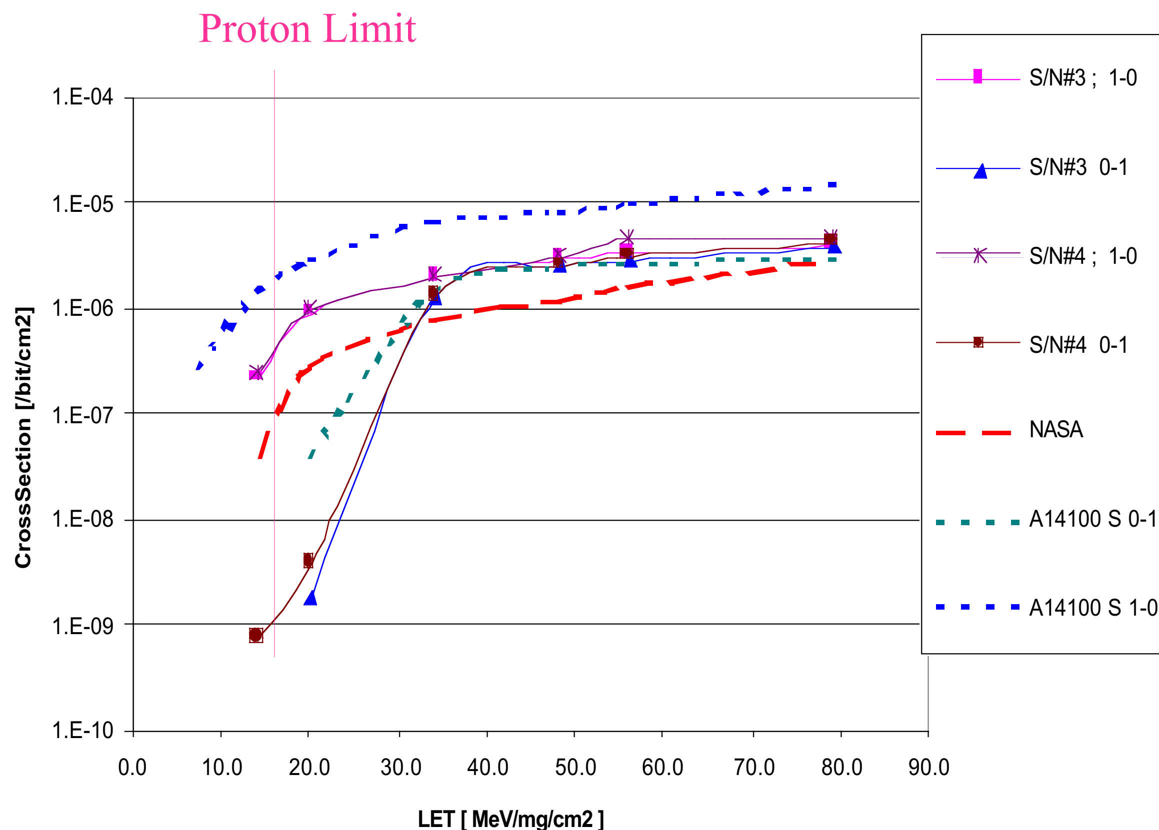
LET (MeV/mg/cm2): 0, 20, 40, 60, 80, 100, 120

Legend: S0, S1, S0, S1

SEU Results
Actel RT54SX16

- 0.6µ Matsushita (MEC)
- "16000 Gates", metal-to-metal
- Logical modules 1452,
  R-cells 528
  C-cells 924,
- User I/O's 177

Obsolete before Qualified

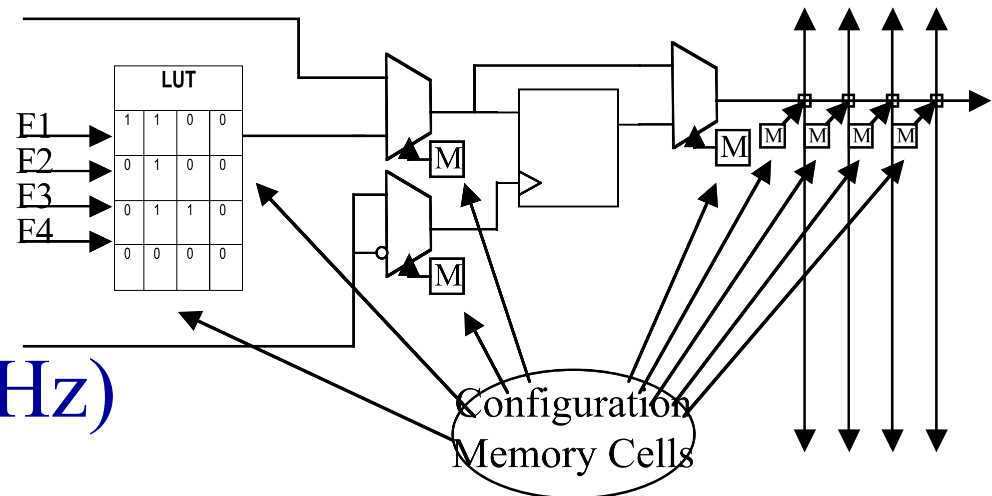


- JTAG - not tested
- 1→ 0 more sensitive than 0 → 1
- A14100A Similar SEU Data
  - 0.8µ ONO Antifuse
- RT54SX Proton SEU similar to A14100A
- Proton SEU 1→ 0 Only

SRAM Based FPGA

SEU Results
Xilinx XQVR300

Xilinx QPRO Virtex
SRAM-based in-system configuration
0,22 µm 5-layer epitaxial process
300k / 600k / 1M System Gates



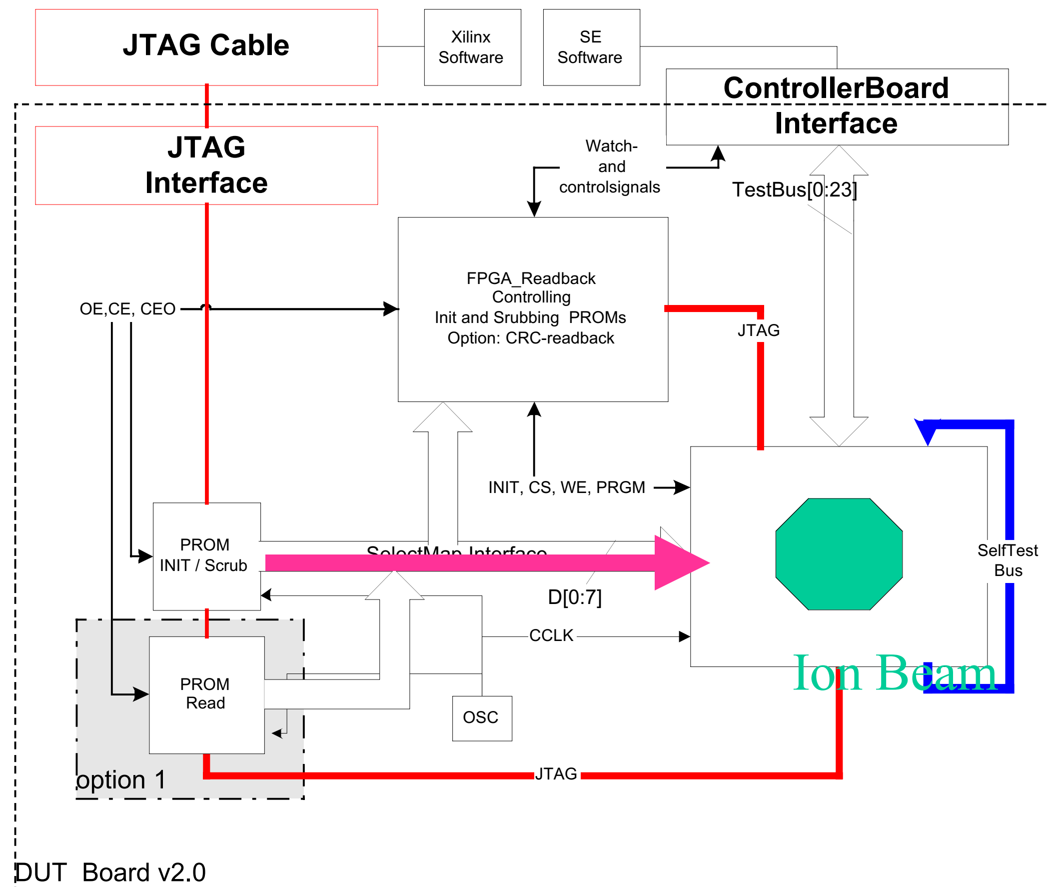
- Dynamic SEE tests (5 MHz)
- Two designs for FF test (user logic)
  - Non Redundant
  - Triple Module Redundant (design by Xilinx)
- Configuration Readback (Bitstream repair)

Configuration Logic

Configuration Readback
Every 10 ms
1465 kbits in XQVR300

Particle flux ~ 1000 ion/cm2

Ion Beam only on chip



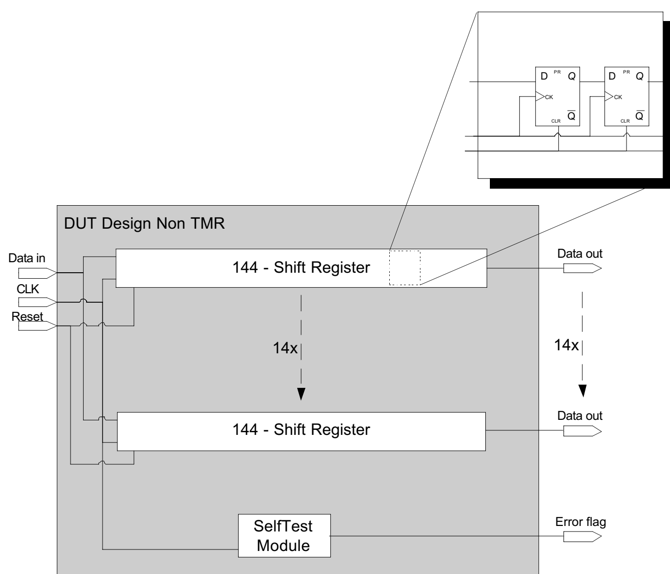
SRAM DUT DESIGN Non-TMR and TMR

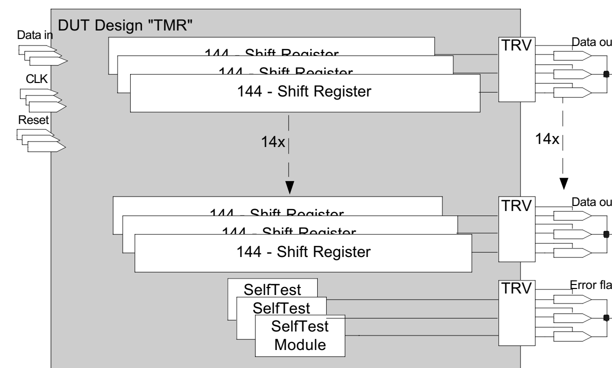
Non-TMR

- 14 Shift-Registers 144 bits long
- 32 % usage of register cells
- Bitstream Readback

TMR

- Same design, triple redundant
- Tripled In- and Outputs
- 98% usage of Register cells
- Bitstream Readback





Detected Error Types

User Logic

Could be Corrected by TMR

"FF", "Dataswap"
SEU in Flip-Flop Registers

Configuration Logic
"Shift Register Failure"
SEU in Configuration Cell causing functional interrupt

Could be Corrected by Re-configuration (Scrubbing + Xilinx TMR)

Architectural Logic

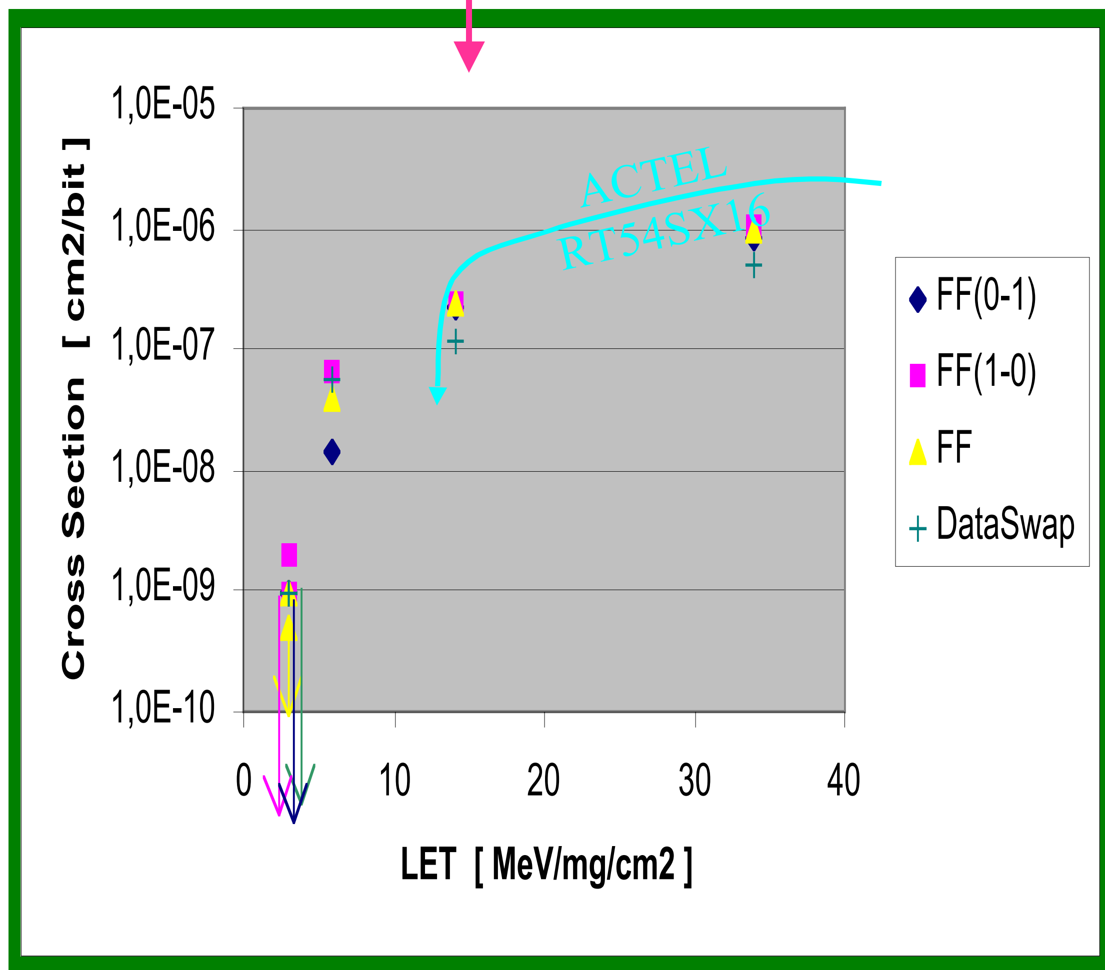
"Local Interrupt Error"

- Reset of Device

Local interrupt of functionality.
SEU in Control Register of Device,

Non Redundant User Logic

Proton



"Static" Error Collection of Register Bits

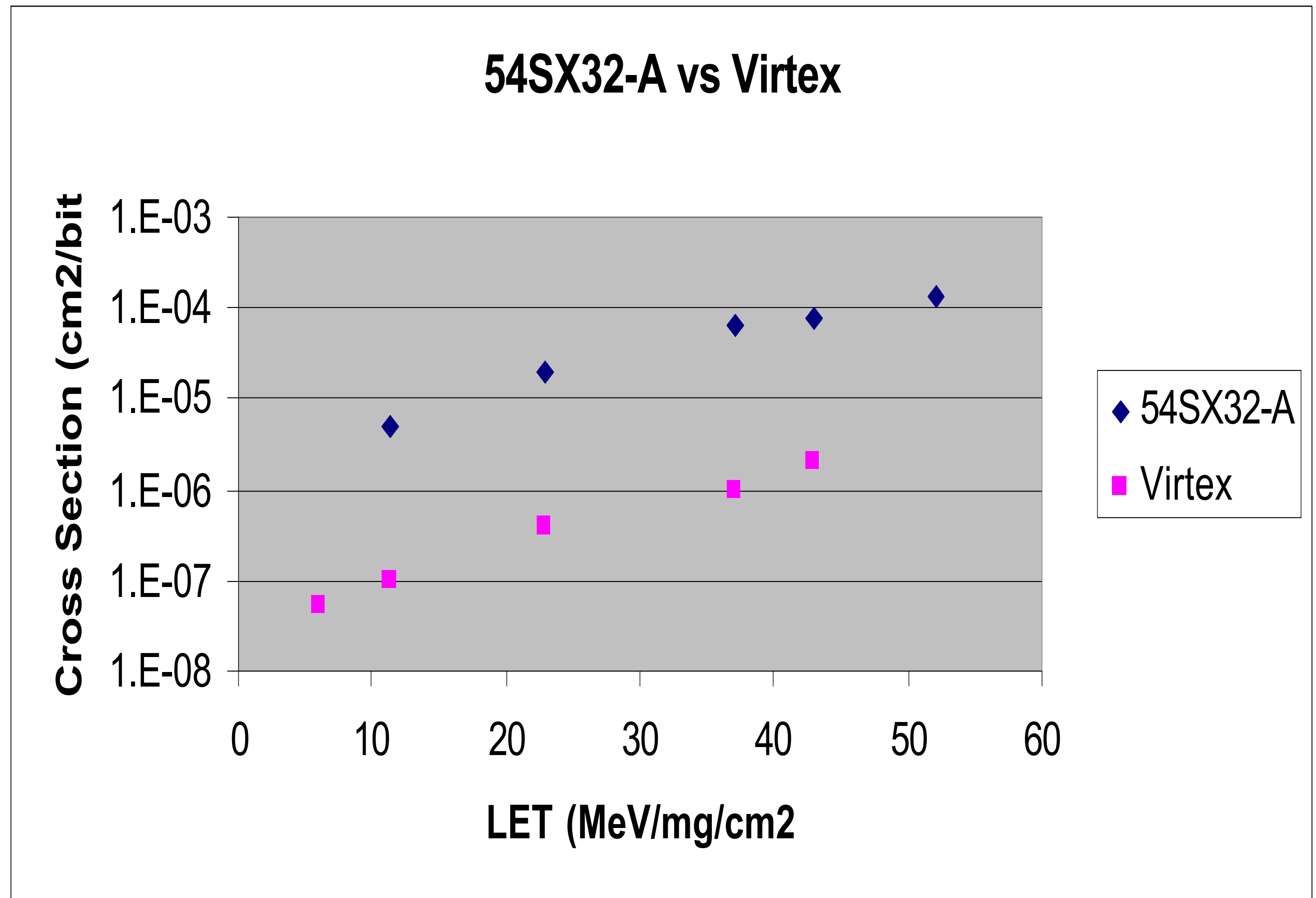
- 1- 0 flip more Sensitive
- DataSwap, "double bit error" Account for 30% of Total
  1 -0 followed by a 0-1
- Proton Sensitive
- Actel & Xilinx ~Sensitivity
  0.8-0.6μ vs 0.25 μ

Two Manufacturer
Same Process

UMC 0.22µ process
(0.25µ)

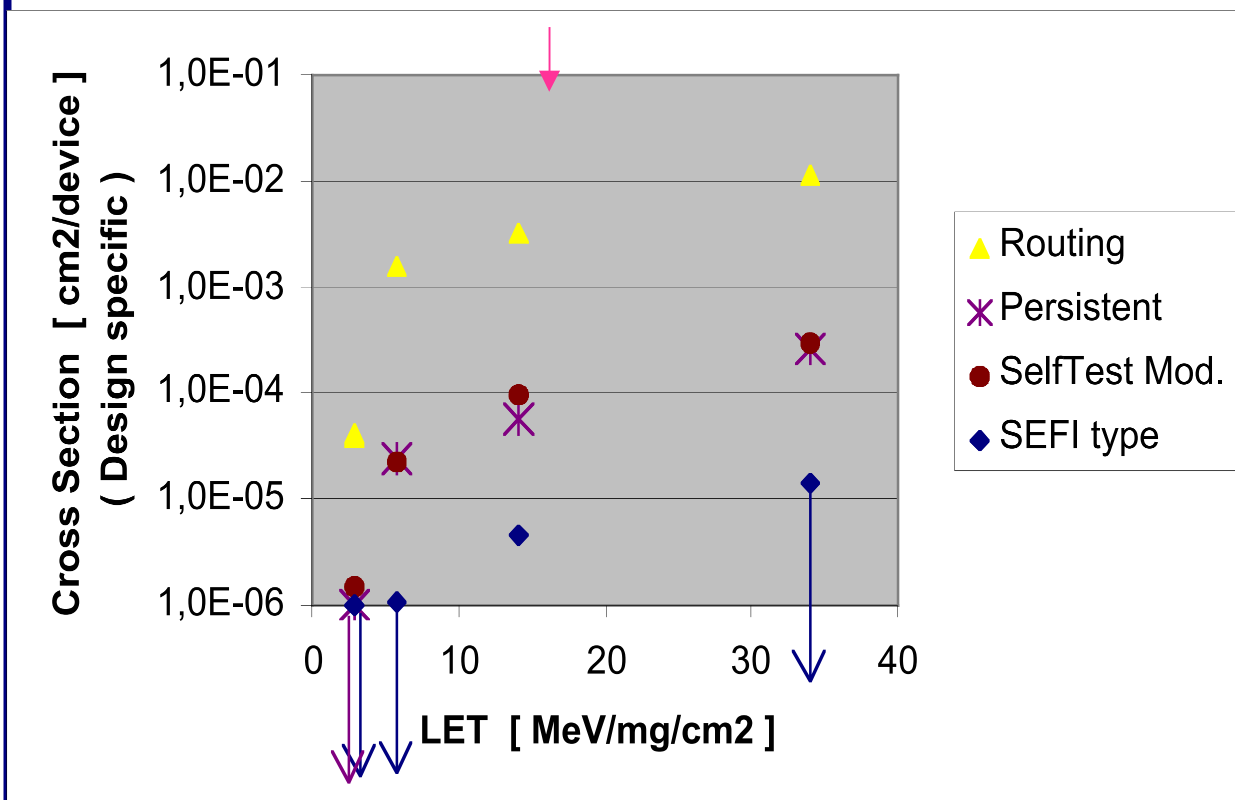
Actel 54SX32-A
vs
Xilinx XQVR300

SEU Data for Registers



Non Redundant Configuration Logic

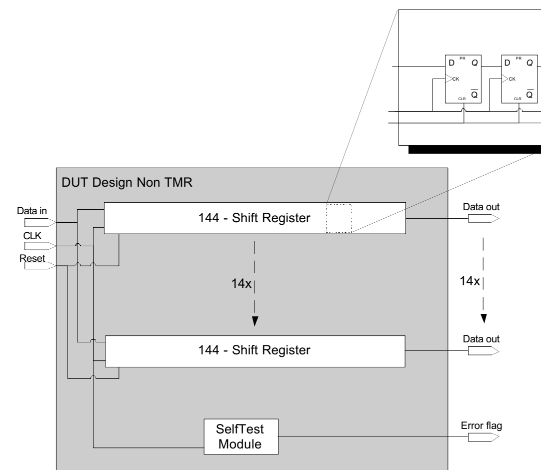
SRAM FPGA



User Logic ~10 times harder

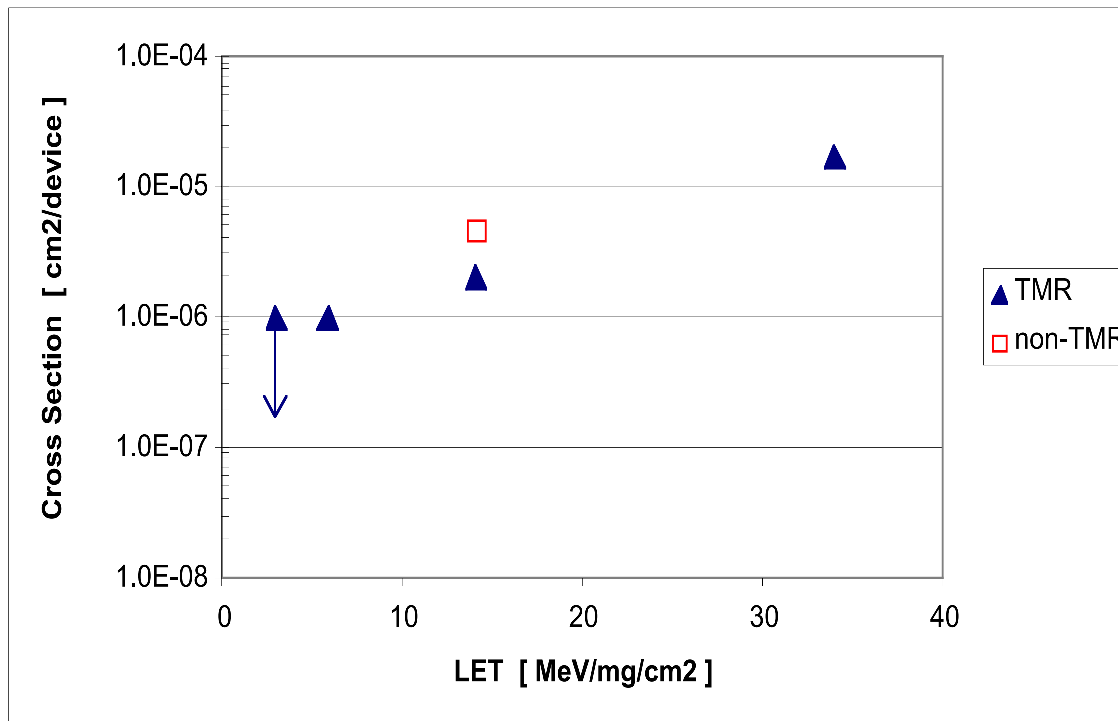
Shift Register Failure

Local Interrupt Error

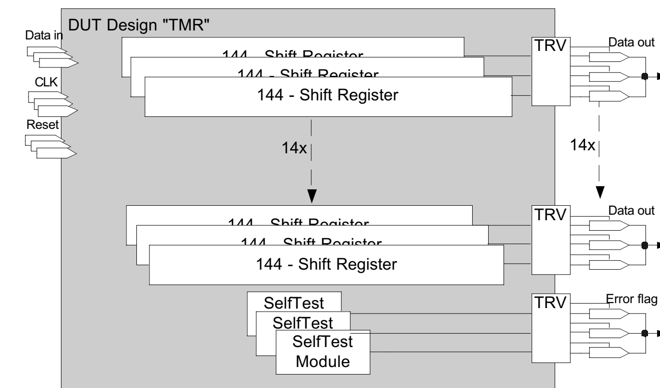


Design Specific

TMR
Configuration logic



- No local interrupt Error
- No User Logic Upset
- One single shift reg error
- Several Functional Failure
  - (control registers)



Proton SEU

Basic Mechanism

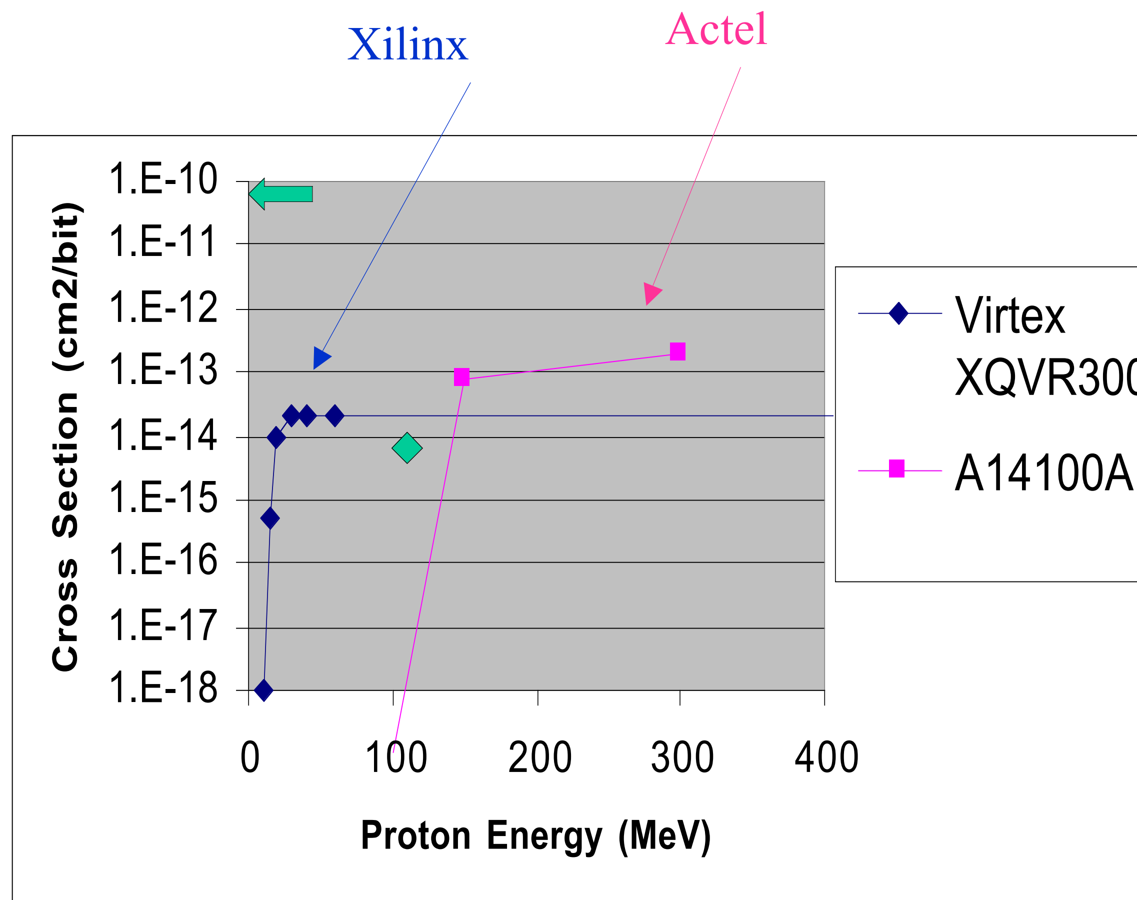
- Nuclear Reaction/ Spallation (p, N) in Close Vicinity of Sensitive Volume
- For Higher Energies, No Difference Between Protons and Neutrons
- For Energies Below 50-100 MeV, Neutrons Give Different Cross Sections (due to (n,n') and (n,α))

Proton SEU Results Xilinx, Actel

Test limit for 0-10 MeV Neutrons (XC4010XL)

100 MeV Neutrons (XC4010)

e+11 Protons
200 MeV = 6 krad(Si)
50 MeV = 17 krad(Si)



Single Event Transients

Technologies smaller than 0.3μ "SEU" in Combinatorial Logic

Glitch from charge particle greater than critical width will propagate through any number of gates

Critical width= inherent delay of the gate

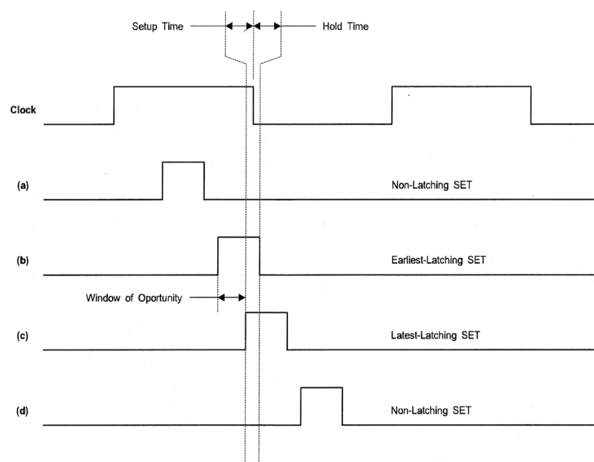
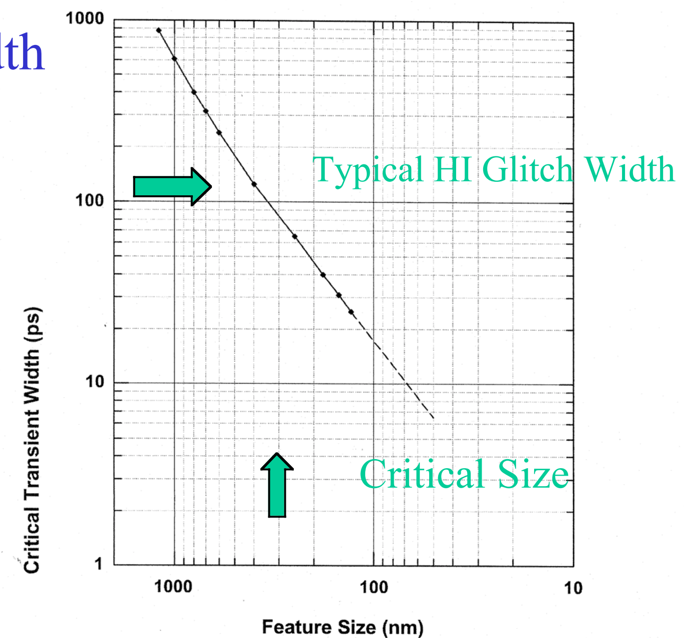


Figure 4. Temporal Relationship for Latching a Data SET as an Error.

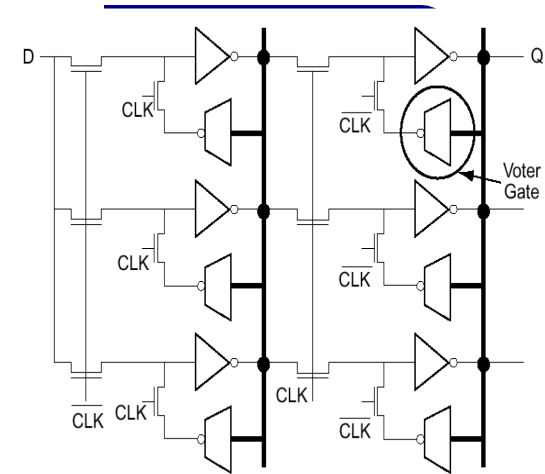


D.G.Mavis and P.H.Eaton, P8111.29

Figure 2. Critical Transient Width vs Feature Size for Unattenuated Propagation.

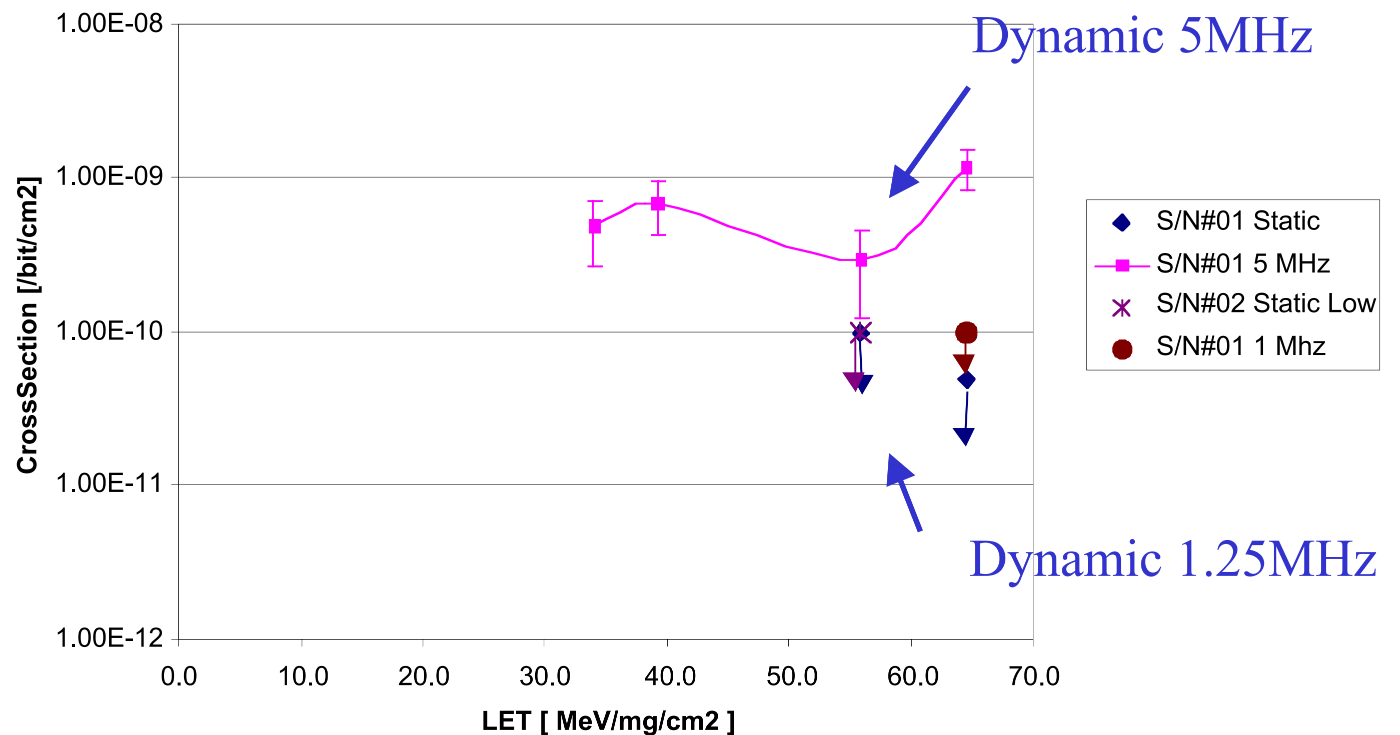
- 0.25µ Matsushita (MEC)
- "32000 Gates", metal-to-metal
- Hard Wire TMR
- Logical modules 2880,
  R-cells 1080
  C-cells 1800,
- User I/O's 228

SEU Results
Actel RT54SX32-S



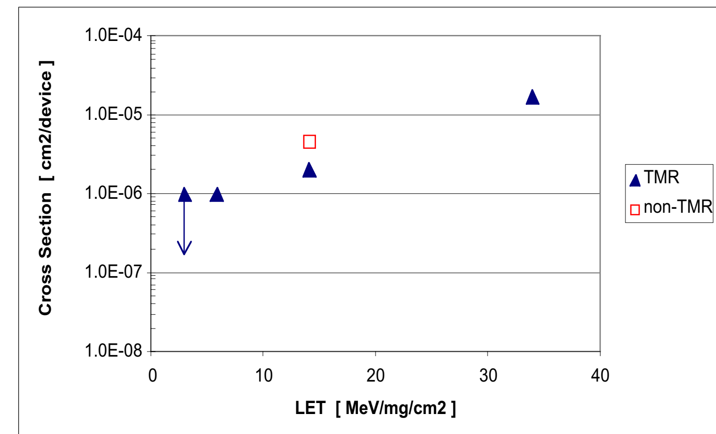
- Single Event Transients Cross Section σ~e-9, (FF σ~e-6)

- No FF SEU
- SET σ~e-9
- SET ~100 MHz in order of FF SEU



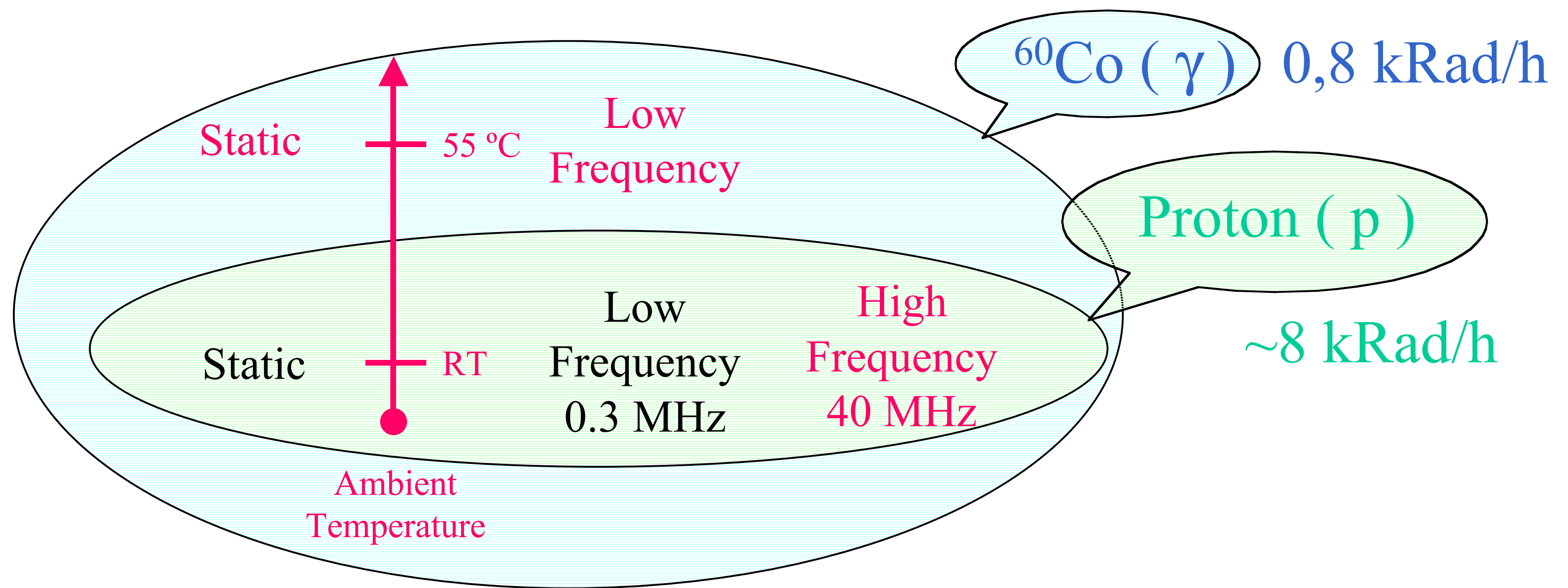
Conclusions

- Complex IC in Radiation Environment - Select with Care
  - Find the Right "COTS",
  - Testing usually needed
- SRAM based FPGA Clearly Interesting
  - \+ Re-configurable
  - \+ Cost per bit
  - \- Very SEU sensitive
  - \- Functional Failure from Charged Particles
  - \- Bitstream Repair May not be a Solution



- Antifuse FPGA - more SEU Safe but Expensive
- Single Event Transients may be Critical for Higher Frequencies

Total Dose Effects by ^{60}Co & Protons



COTS Total Dose Response

Source:

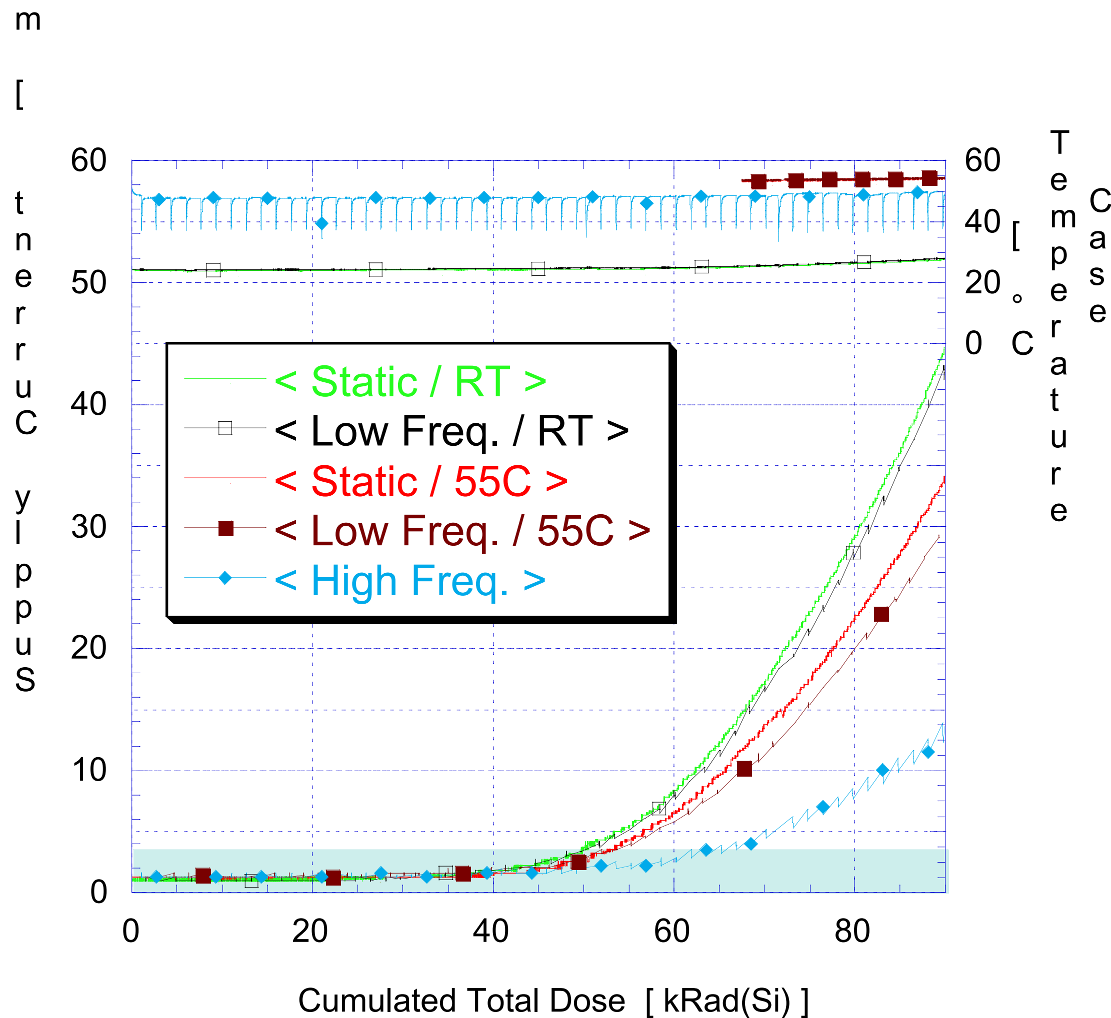
- ^{60}Co

TID Conditions:

- Static /Low Frequency (25ºC)
- Static /Low Frequency (55ºC)
- High Frequency (~ 50ºC)

Parameter:

- Standby Current
- Case Temperature

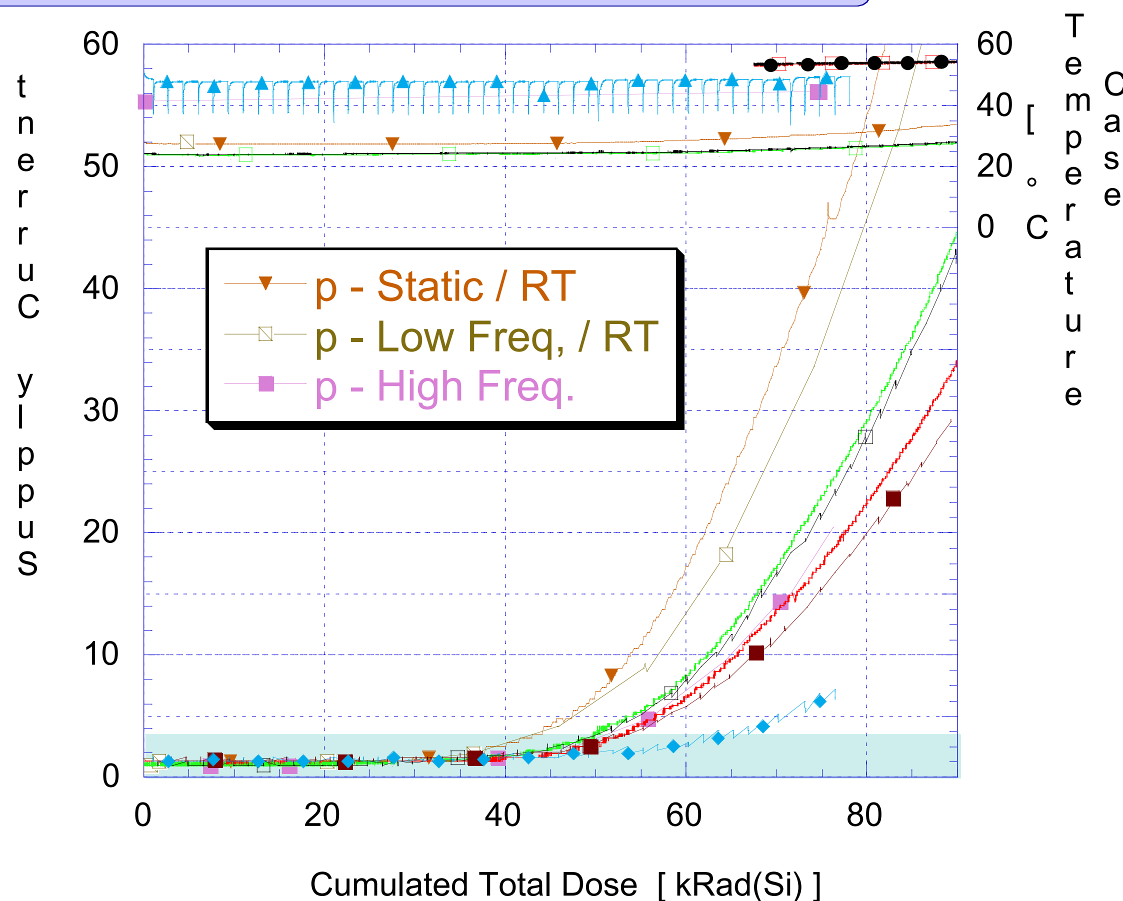


Proton Total Dose Response

Source:
- Proton, 100 MeV

TID Conditions:
- All 3 Tests at Room Temp.

Parameter:
- Standby Current
- Case Temperature



Similar behavior as for Cobolt-60

Xilinx Total Dose Response

Manufacturer Guarantee 100 krad

Testing indicate
Power off/on Problem at