Status of the CARIOCA Project

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Abstract

CARIOCA is an amplifier shaper discriminator chip, developed in IBM 0.25μm CMOS for the readout of the LHCb muon wire chambers. Four prototype chips were designed and fabricated over the last two years with a step by step approach testing the different functionalities of the chip. In this paper the design and test results of a positive polarity and negative polarity amplifier, as well as a shaper circuit, are discussed.

I. INTRODUCTION

The LHCb muon system will use 80,000 wire chamber channels of negative (wire readout) and positive (cathode readout) polarity. Figure 1 shows the block diagram for one readout channel.

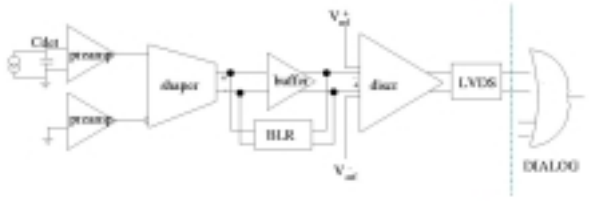

Figure 1: Block diagram of one readout channel

The chamber signal, with a fast rising edge and a long 1/t tail, is amplified and shaped to a unipolar narrow pulse in order to cope with the high rate expected in the experiment. A baseline restoration circuit is needed to compensate for baseline shifts and fluctuations. The circuit is fully differential from the shaper on.

To this date the positive and negative amplifiers as well as shaper and discriminator have been designed and fabricated. The results of a 4-channel version of the positive polarity amplifier are presented in [1], together with the chip specifications. In this report we present measurements of a 14-channel positive amplifier chip and results of the negative polarity amplifier and the shaper.

II. THE 14-CHANNEL POSITIVE POLARITY AMPLIFIER

The main purpose of the 14-channel chip was to test chip uniformity and crosstalk. The individual channels show linearity up to an injected charge of 200fC (delta input), with a non-linearity error of about 1%. The measured sensitivity is 8mV/fC up to a detector capacitance of 140pF and we find an equivalent noise charge of ENC=867e^- + 36e^-/pF. The sensitivities of all 14-channels were found to be within 10%. The noise and threshold variation was measured to be 7% R.M.S. The crosstalk is smaller than 1%. The power consumption of about 18mW per channel is dominated by LVDS driver.

III. THE NEGATIVE POLARITY AMPLIFIER

A. Design

The design of the negative polarity amplifier follows closely that of the positive one [1]. Figure 2 shows a simplified schematic. The input stage is a cascode structure (N1) with a large input transistor that is followed by a voltage to current converter (N0) and a current mirror (N2). The mirror feeds the current to the output stage (N4) and back to the input stage. The output current is finally converted into voltage that is driven to the chip pad by an analog buffer. The size of the transistors N3 and N4 determines the current gain of about 6.

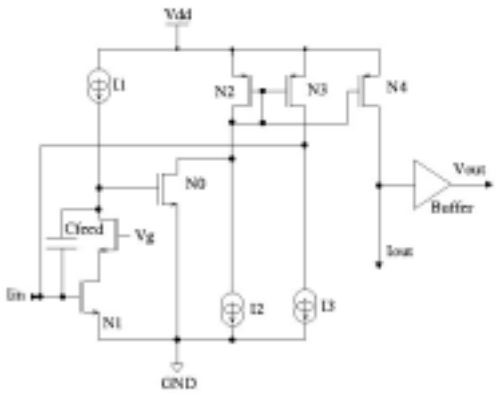

Figure 2: Simplified schematic of the negative polarity amplifier.

From CADENCE simulation the bandwidth was found to be 16MHz and 23MHz for the negative and positive amplifier, respectively. The input impedance is below 50Ω within the bandwidth.

B. Measurements

The circuit displays linearity within 1% up to 200fC. Results of peaking time, sensitivity and noise measurements vs. detector capacitance, together with CADENCE simulation, are shown in Figure 3, 4 and 5,.
The fit to the points of figure 5 gives a noise of ENC=951e-+31e-/pF.

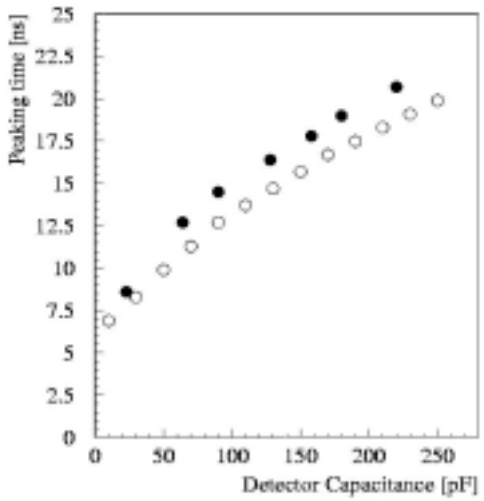

Figure 3: Measured (black dots) and simulated (white dots) peaking time vs. detector capacitance for the negative polarity amplifier.

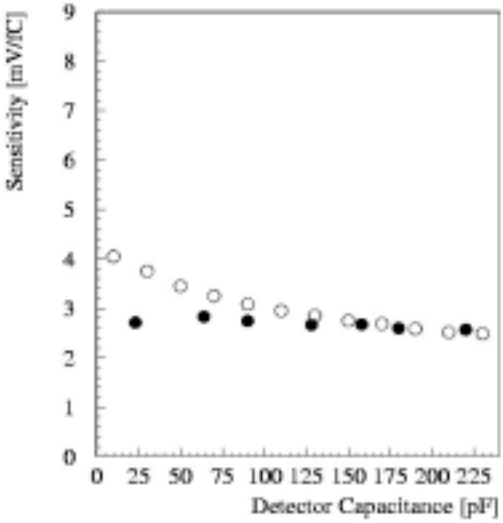

Figure 4: Measured (black dots) and simulated (white dots) sensitivity vs. detector capacitance for the negative polarity amplifier.

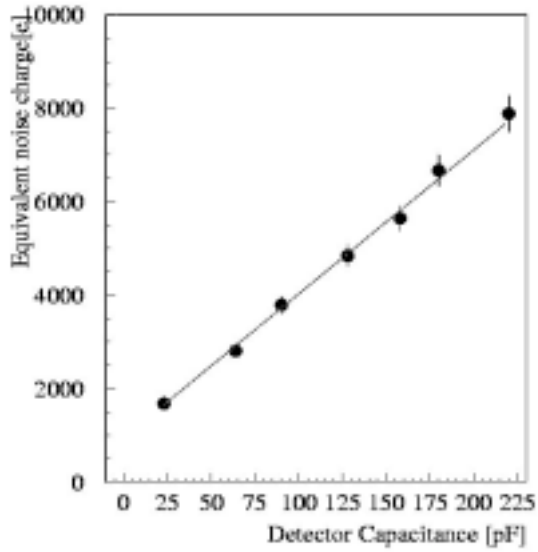

Figure 5: Measured equivalent noise charge vs. detector capacitance for the negative polarity amplifier.

IV. THE SHAPER

C. Design

The shaper is a differential amplifier in a folded cascode configuration with common mode feedback. A simplified schematic is shown in Figure 6. The shaper is designed with a speed such that the amplifier peaking time is not significantly degraded. Therefore the dominant high frequency pole is located at 160MHz. The 1/t tail cancellation is performed by a double pole/zero compensation network [2][3] displayed in Figure 7.

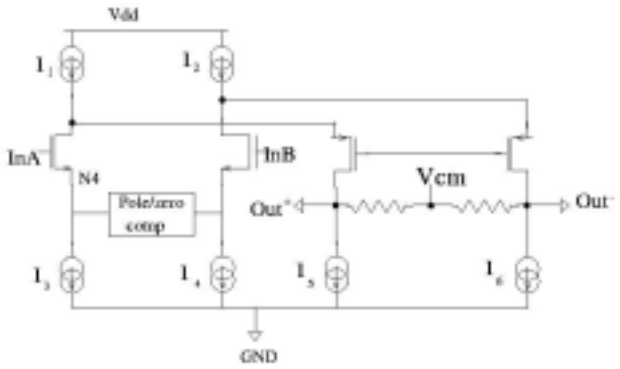

Figure 6: Simplified schematic of the shaper circuit.

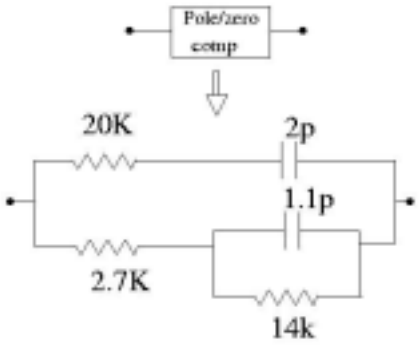

Figure 7: Schematic of the pole/zero compensation network.

D. Measurements

The prototype chip uses two positive polarity amplifiers followed by the shaper. The differential shaper output was equipped with two analog buffers and only one of them was read out during the tests.

Figure 8 and 9 show the measured peaking time and noise versus detector capacitance for two different bias currents configurations. For high bias current a noise performance of ENC=1290e-+40e- is achieved.

The offset ENC is higher than that of the positive amplifier alone due to the presence of two amplifiers at the shaper input. The slope is consistent with that of the positive amplifier chip but higher than that of the negative amplifier due to the large bandwidth of the shaper.

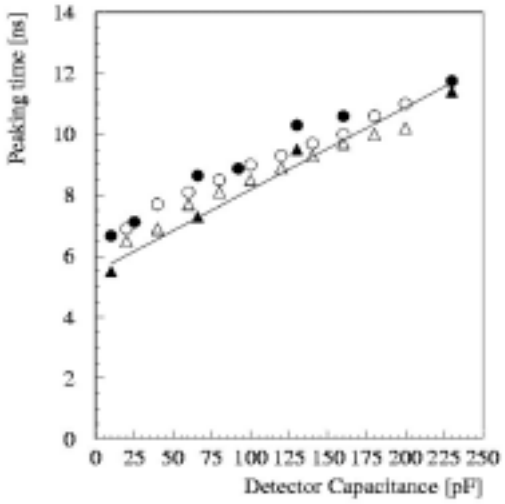

Figure 8: Measured (black symbols) and simulated (white symbols) peaking time of the shaper chip as a function of detector capacitance for a delta input. The triangles and dots correspond to two different bias current configurations.

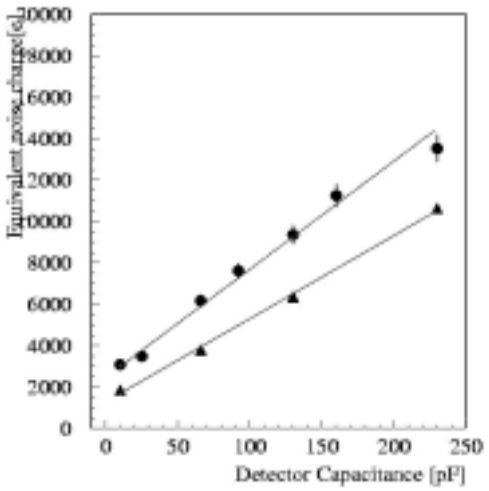

Figure 9: Measured equivalent noise charge of the shaper chip as a function of detector capacitance. The triangles and dots correspond to two different bias current configurations.

A quasi-1/t current injector, realised with four parallel RC circuits, was used to simulate a detector pulse. Figure 10 shows the output pulse from the negative amplifier and displays a long tail. Figure 11 shows the output pulse from the shaper with the same time scale of Figure 10 indicating that the tail is to large extent suppressed.

Figure 12 shows the peaking time versus detector capacitance with the 1/t injector.

The pulse width (at 20% amplitude) was found to be less than 30ns after shaping up to 200pF detector capacitance.

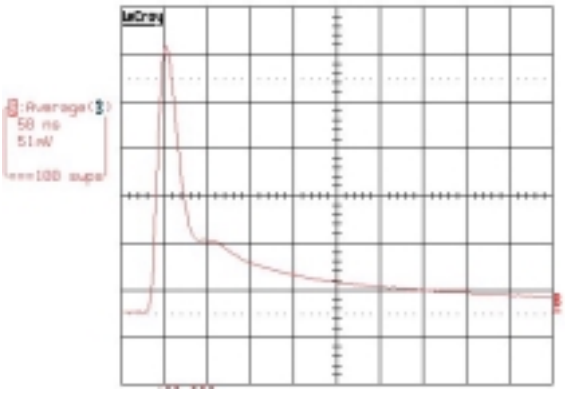

Figure 10: Output of the negative polarity amplifier for a 1/t current pulse input.

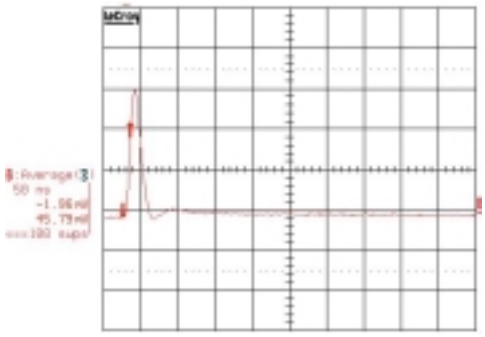

Figure 11: Shaper output for a 1/t current pulse input.

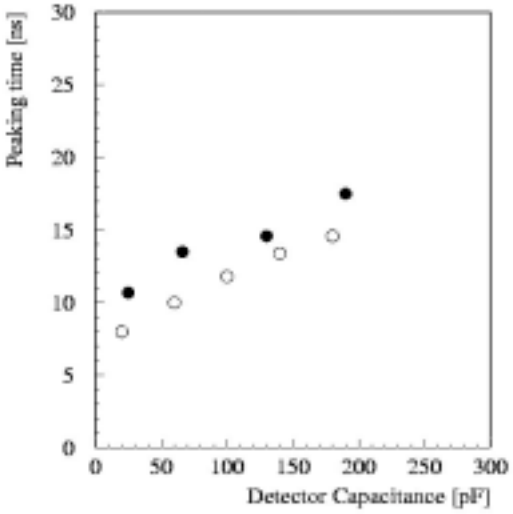

Figure 12: Measured (black dots) and simulated (white dots) peaking time of the shaper chip as a function of detector capacitance for a 1/t current pulse input.

V. Conclusions and Future Plans

Four prototype chips of the CARIOCA front-end have been produced during the last two years. Positive and negative amplifier and shaper circuits were tested and their characteristics satisfy the requirements for operation in LHCb. A final prototype, including a baseline restoration circuit, will be submitted in November 2001. The overall goal is to start chip production by the end of 2002.

VI. Acknowledgement

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VII. References

[1] D.Moraes, "CARIOCA – a fast binary front-end implemented in 0.25um CMOS using a novel current-mode technique for the LHCb Muon detector", presented at LEB2000.

[2] R.A.Boie et al., "Signal shaping and tail cancellation for gas proportional detectors at high counting rates", Nucl. Instr. and Meth. 192 (1982) 365.

[3] M. Newcomer, "Progress in development of the ASDBLR ASIC for the ATLAS TRT", presented at LEB1999.