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The CMS HCAL Data Concentrator: A Modular, Standards-based Design

A Review of the CMS HCAL DAQ

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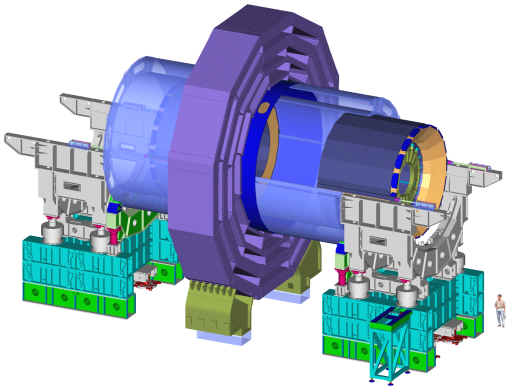

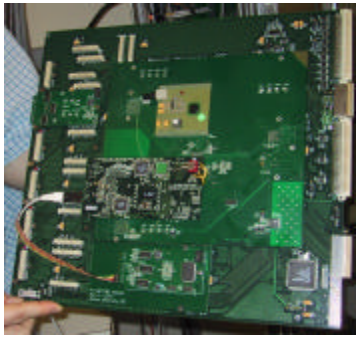

Outline

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- HCAL Trigger DAQ Overview
  - Requirements
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  - DAQ Crate
- HCAL Trigger Readout Card (HRC)
  - Requirements
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- HCAL Readout Controller (HRC)
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HCAL Trigger/DAQ Requirements

- Digitize scintillator pulses every BX
  - Pulses occupy ~3 BX periods (25ns each)
  - Dynamic range required is about 10^4 (14-15 bits)
  - QIE (custom floating point ADC) used
- Reliably assign energy measurement to a single BX for Level 1
  - F.I.R. filter implemented in FPGA (ala FERMI)
  - Synchronized across HCAL+ECAL for input to Level 1
- Transmit data to DAQ on L1A
  - Zero Supression
  - Formatting

HCAL FE/DAQ Overview

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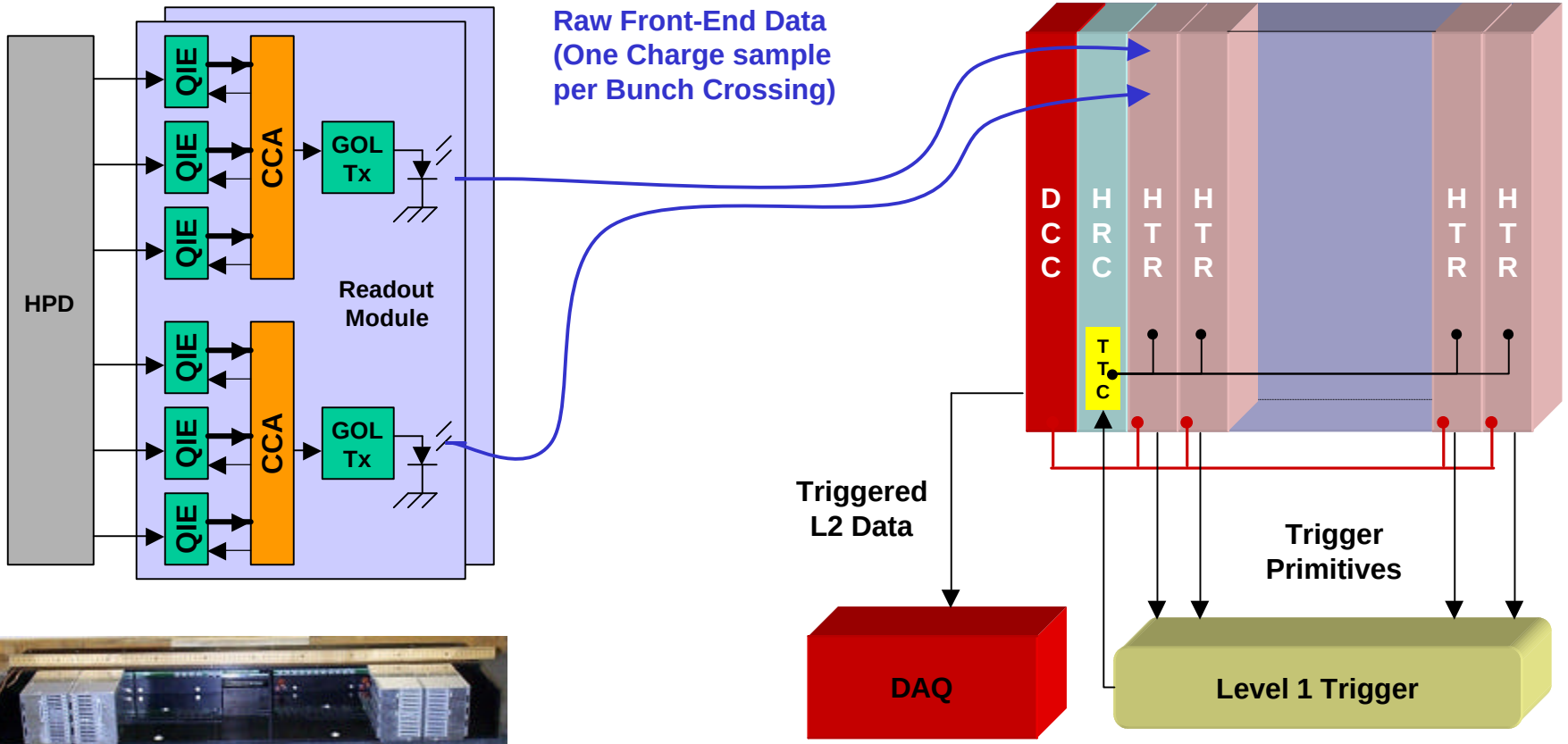
Readout Box (RBX)
(On detector)

DAQ Crate
(in UXA)



HCAL Channel Counts

Region	Towers	GOL Fibers	Trigger Towers	Crates
Barrel	2,160	720	2,160	6
Outer	2,160	720	0	6
Endcap	2,160	720	1,728	2
Forward	2,016	672	144	6
Overlap	864	288	144	6
Total	**9,360**	**3,120**	**4,176**	**26**

HCAL DAQ Crate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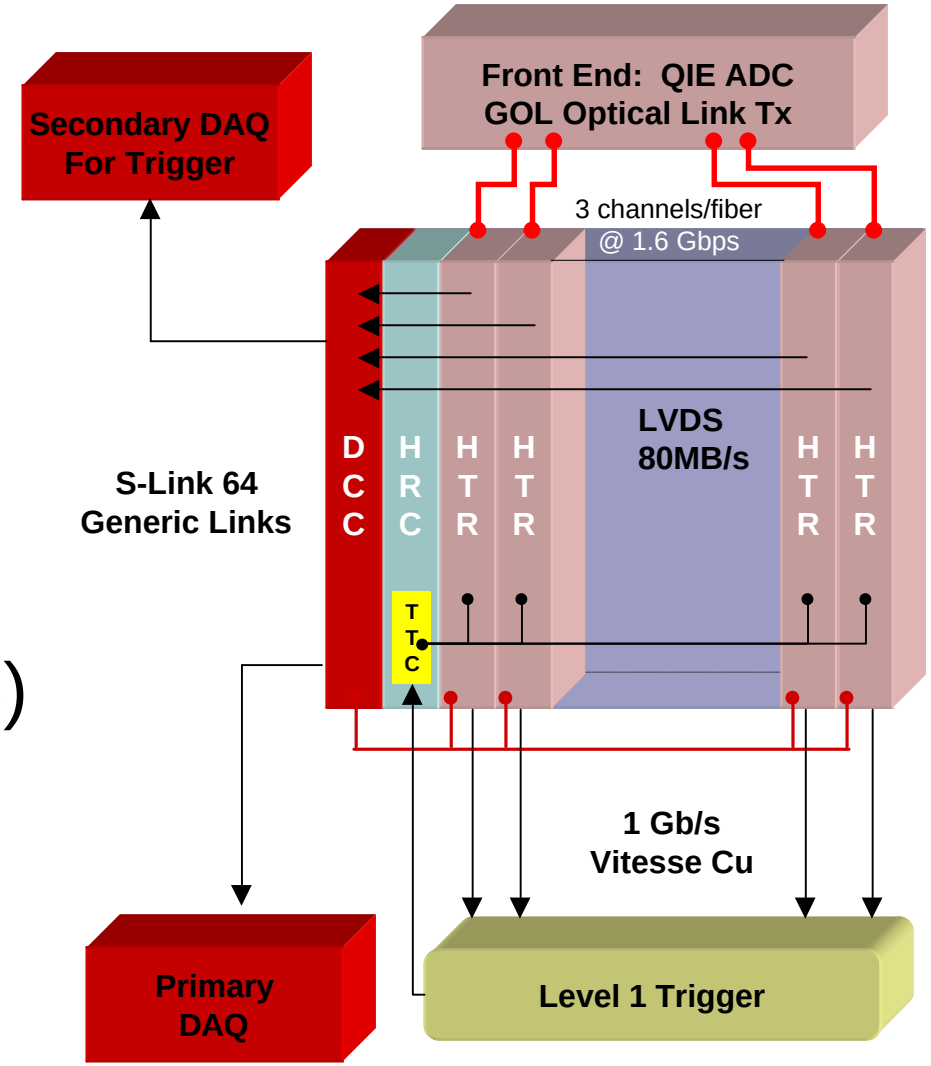
- 9U x 400 VME64x Crate
- Controller (HRC)
  - Commercial CPU/Bridge
  - TTC Fanout
- Readout Cards (HTR)
  - Front-end data in (GOL)
  - Level 1 Out (Vitesse Cu)
  - Level 2 Out (LVDS)
- Data Concentrator (DCC)
  - Level 2 in (LVDS) x 18
  - S-Link Out x 2



HCAL Trigger Readout Card (HTR)

- Level 1 (Trigger) Path
  - Energy Sum and Bunch Crossing Determination
  - Output Trigger Primitives to Level 1 synch'd to BX
- Level 2 (DAQ) Path
  - Zero-supress Level 2 data (energy filter)
  - Package raw data plus trigger primitives
  - Send to Data Concentrator every L1A
- Implementation
  - FIR filter for bunch crossing (ala FERMI)
  - Single large FPGA for core logic

HCAL Trigger Readout Card

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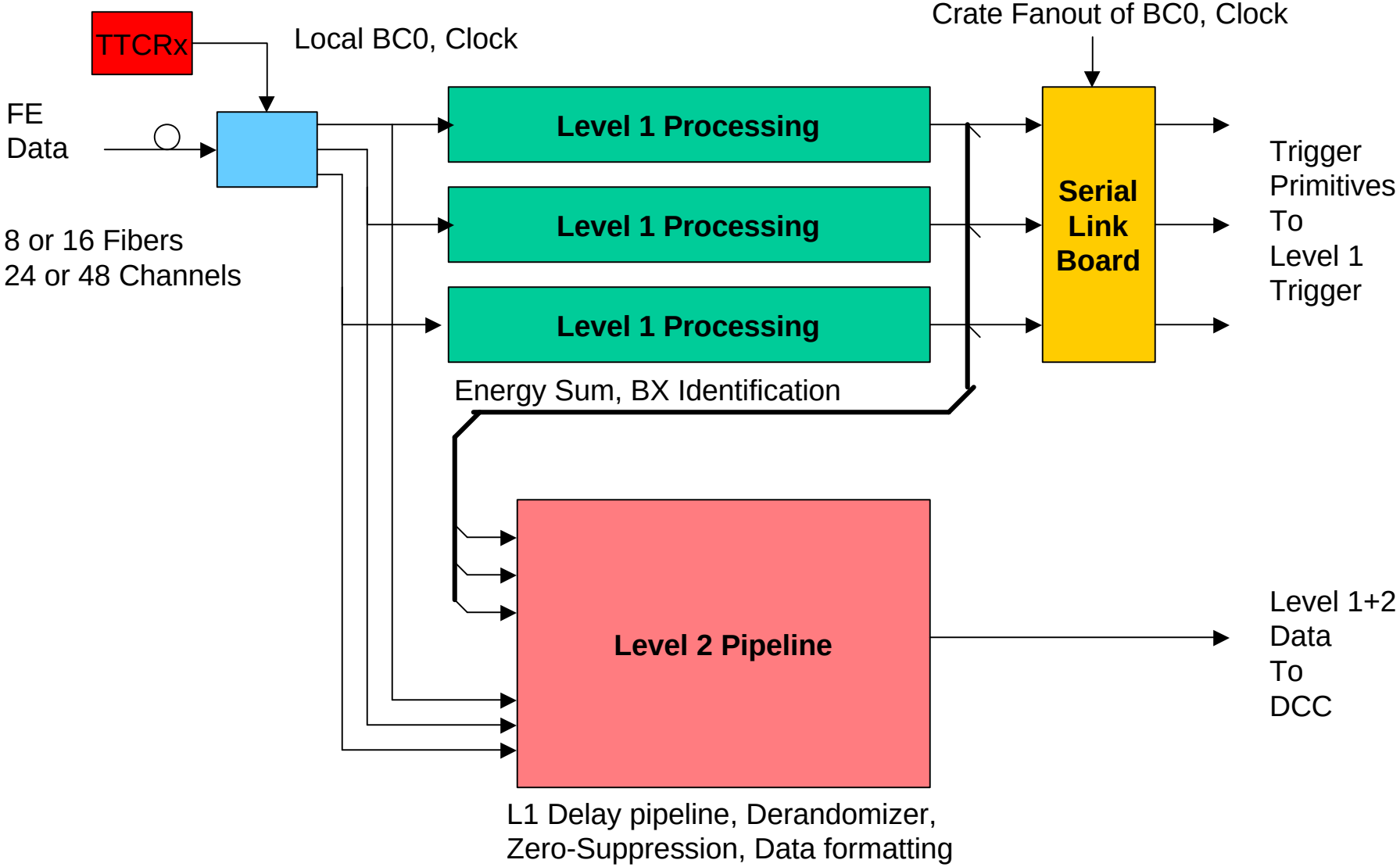

HCAL Trigger Readout Card

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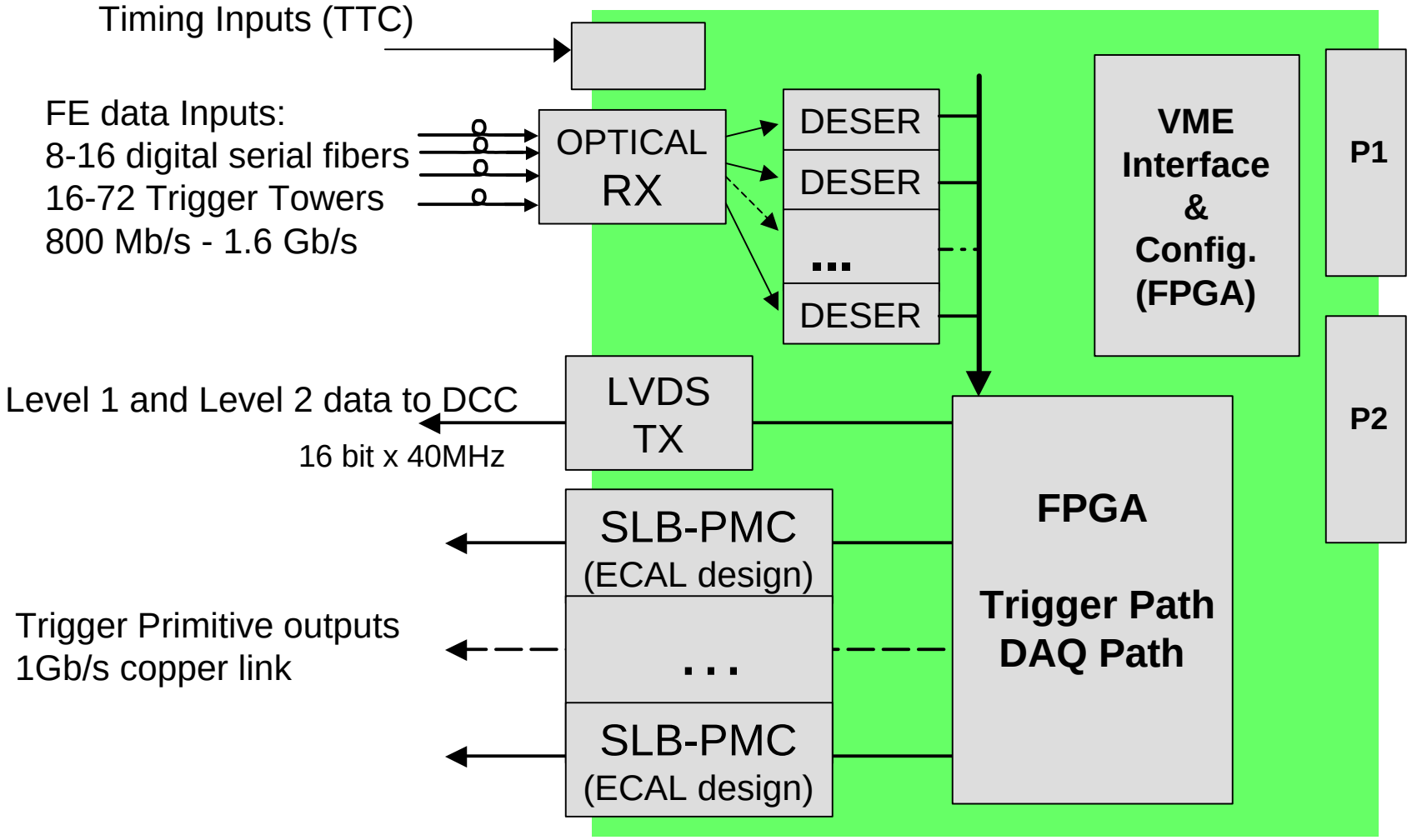

HTR Demonstrator Board

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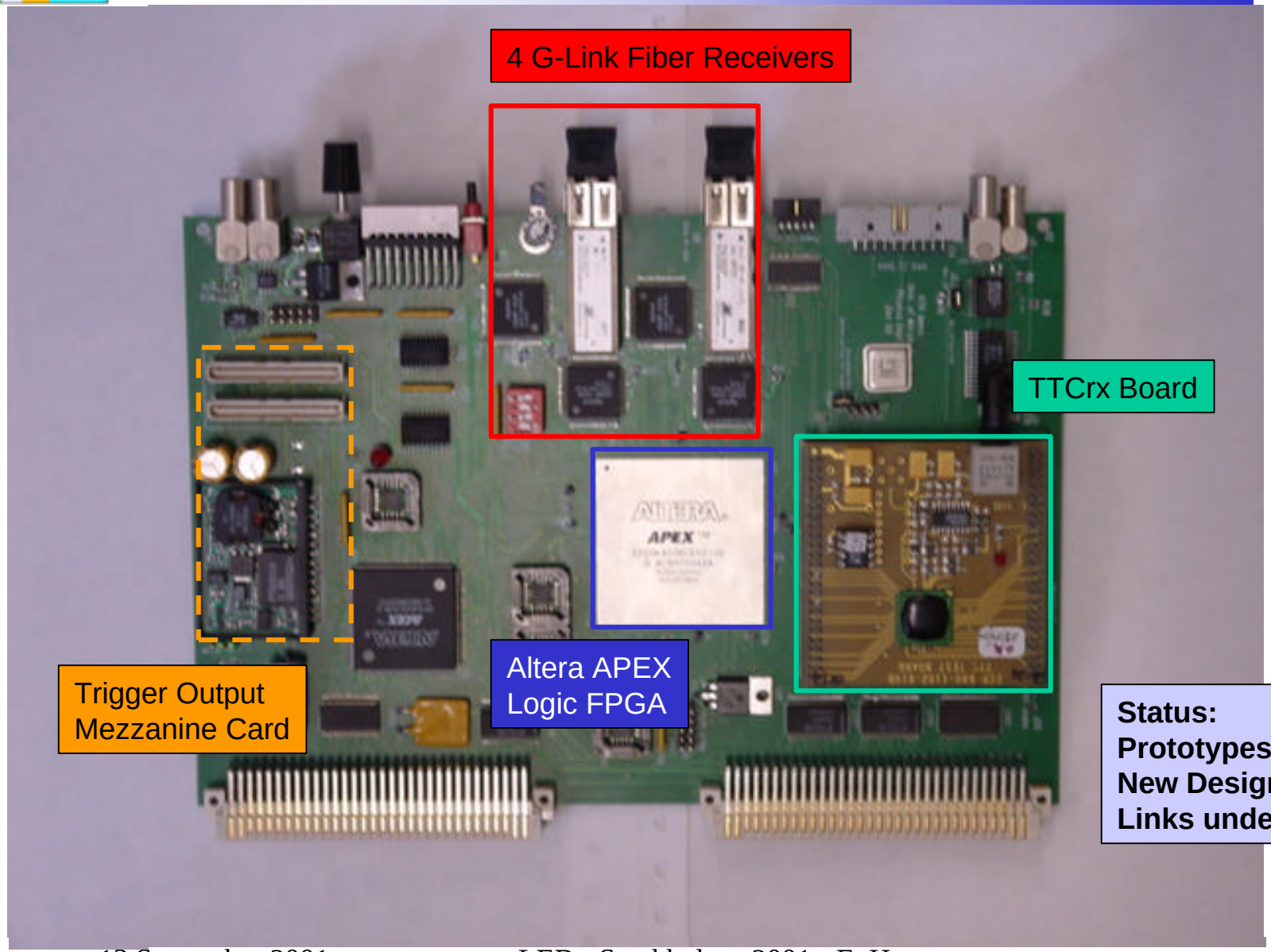

Status:
Prototypes Built/Tested
New Design using GOL
Links underway

HCAL Data Concentrator

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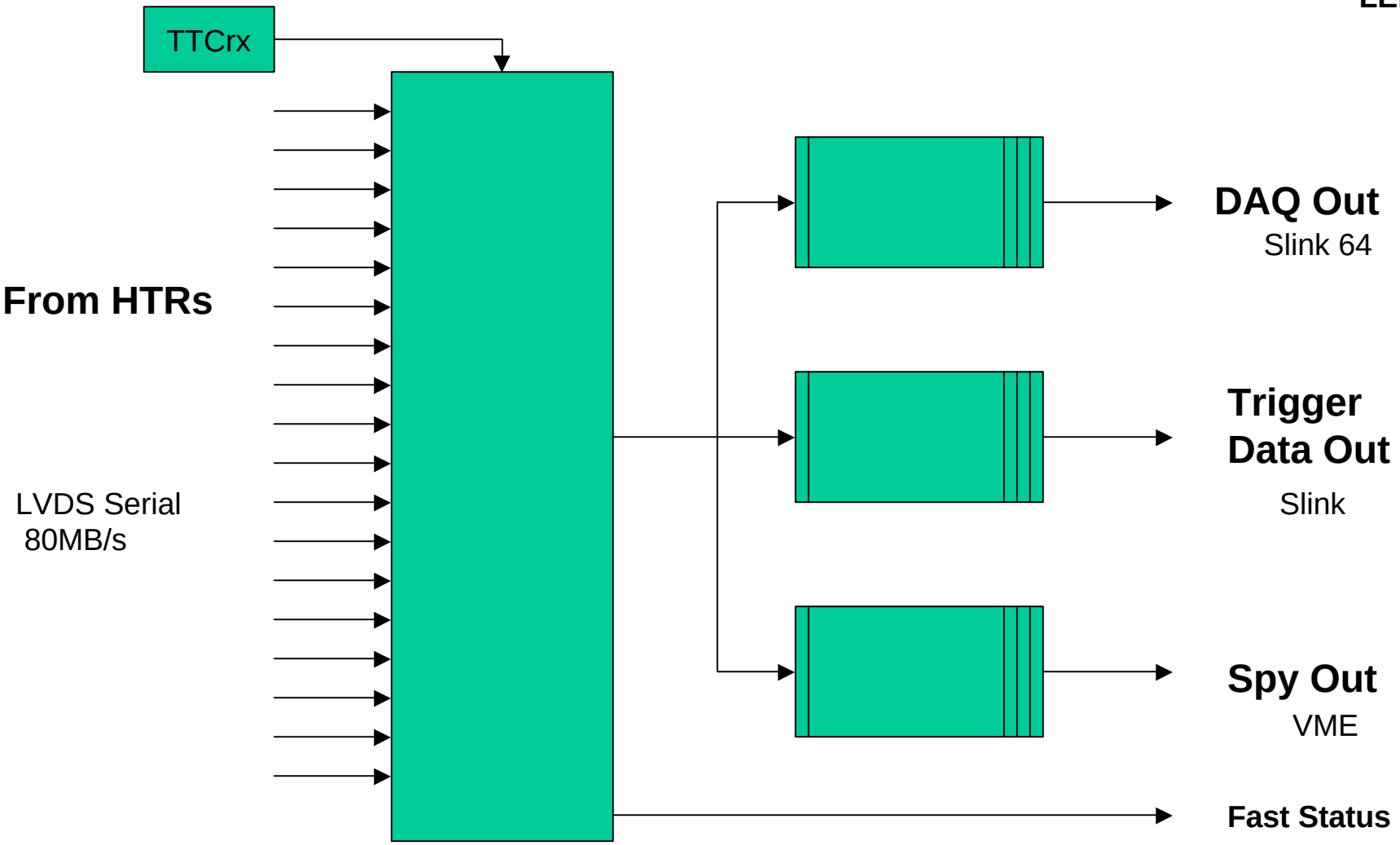

HCAL DCC Prototype Architecture

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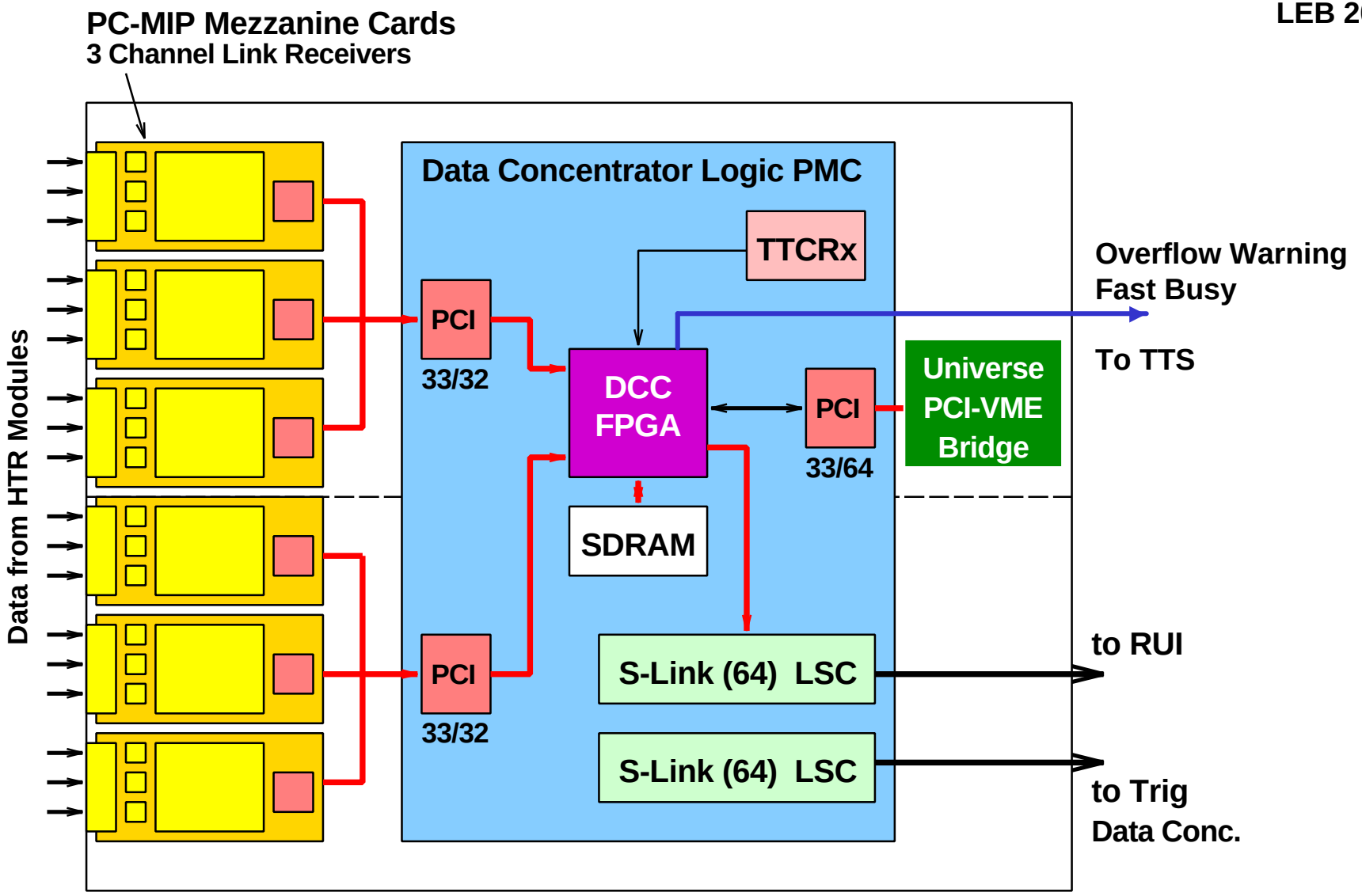

HCAL DCC Motherboard

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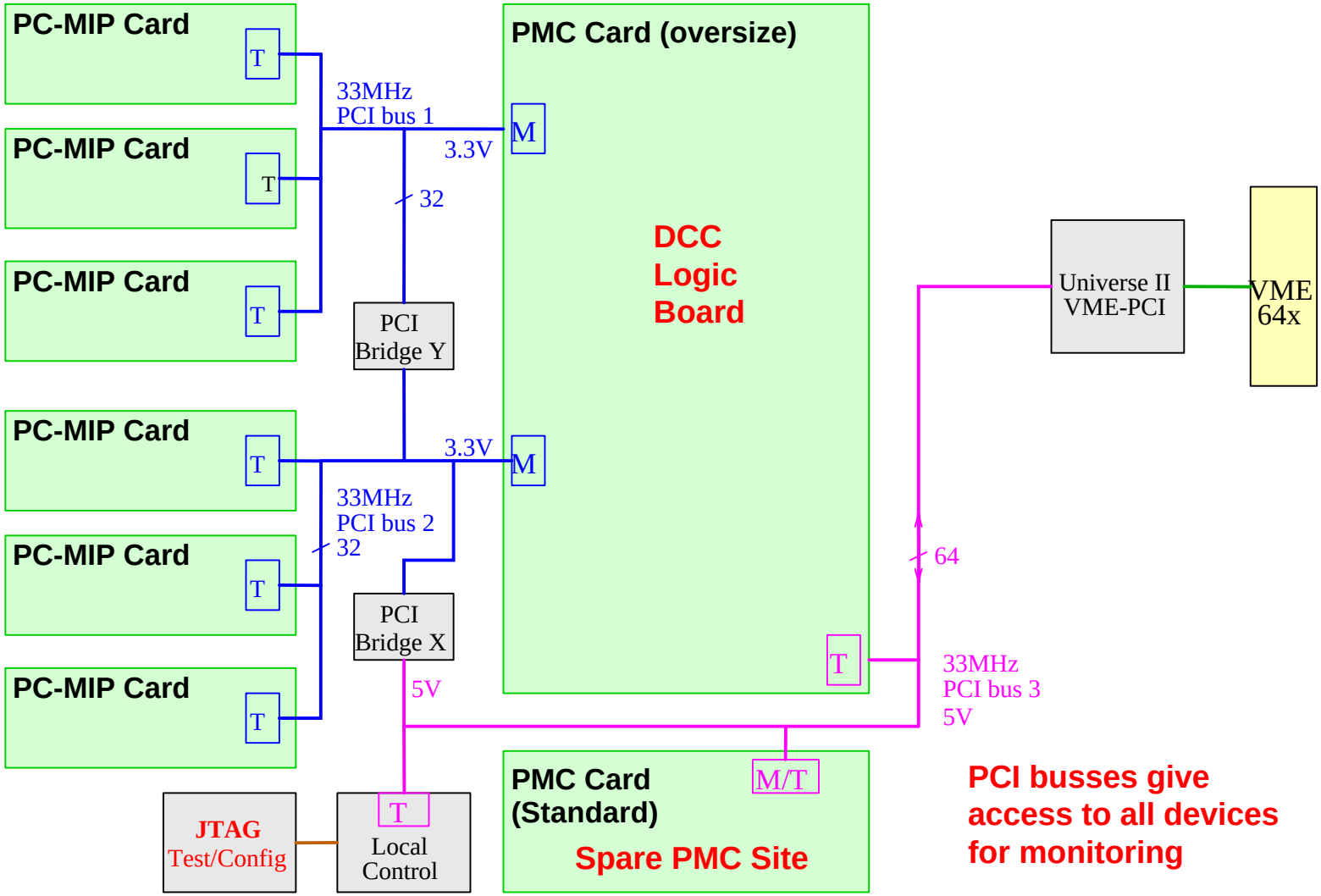
3-Channel LVDS Receivers



PCI busses give access to all devices for monitoring

HCAL DCC Motherboard

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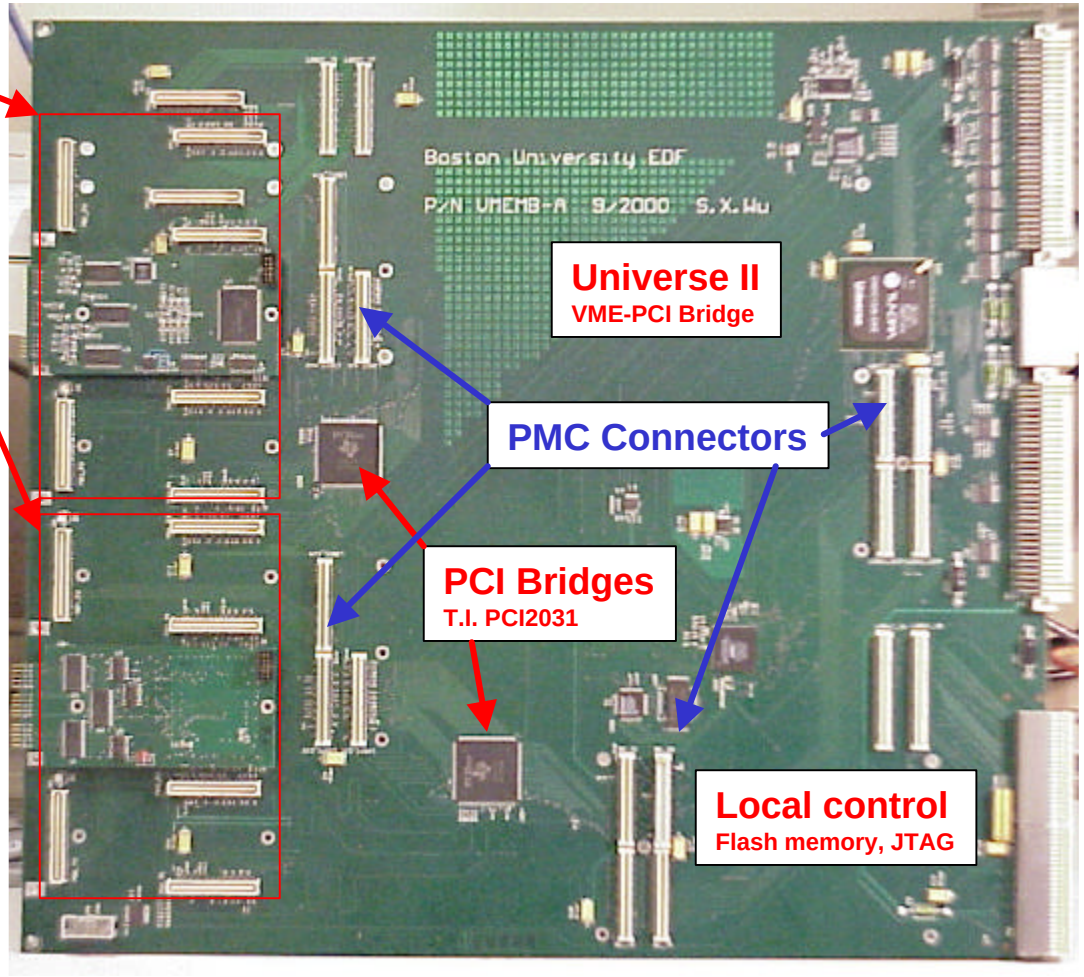

Status:
10 Produced and Tested.
No known problems

PC-MIP 3 Channel Link Receiver

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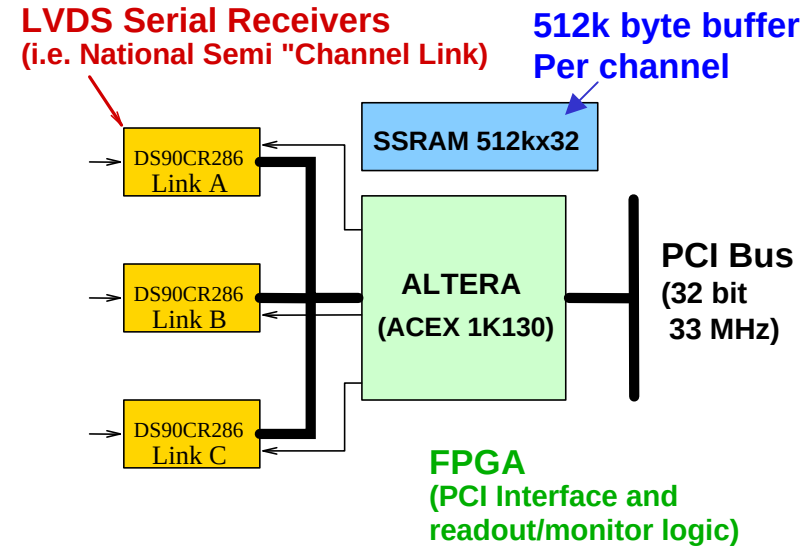
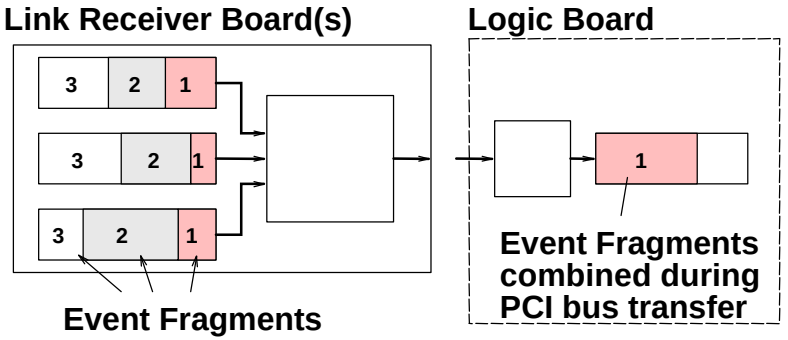
- 3 “Channel Link” LVDS receivers
- PCI target interface
- On-board logic:
  - ECC (Hamming) plus parity
    - Correct 1-bit, detect multi-bit errors
  - On-the-fly Event Building
  - Event number checking
  - Overflow warning (discard data payload on overflow)
  - Missing header/trailer detection & repair
  - Monitoring:
    - Count of words, events, errors
    - Status update on “marked” event for synchronization of monitoring
  - Status: 20 second-generation prototypes build (design is done)





PC-MIP 3-Channel Link Receiver

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Altera ACEX FPGA
EP1K100FC484-1

PC-MIP Interface
(PMC 33MHz 32 bit)

Programming Connector
For flash memory

MT55L512V ZBT
512Kx32 SSRAM

DS90CR256A
Channel-Link RX

Cypress Clock
Multipliers

DCC Logic Board

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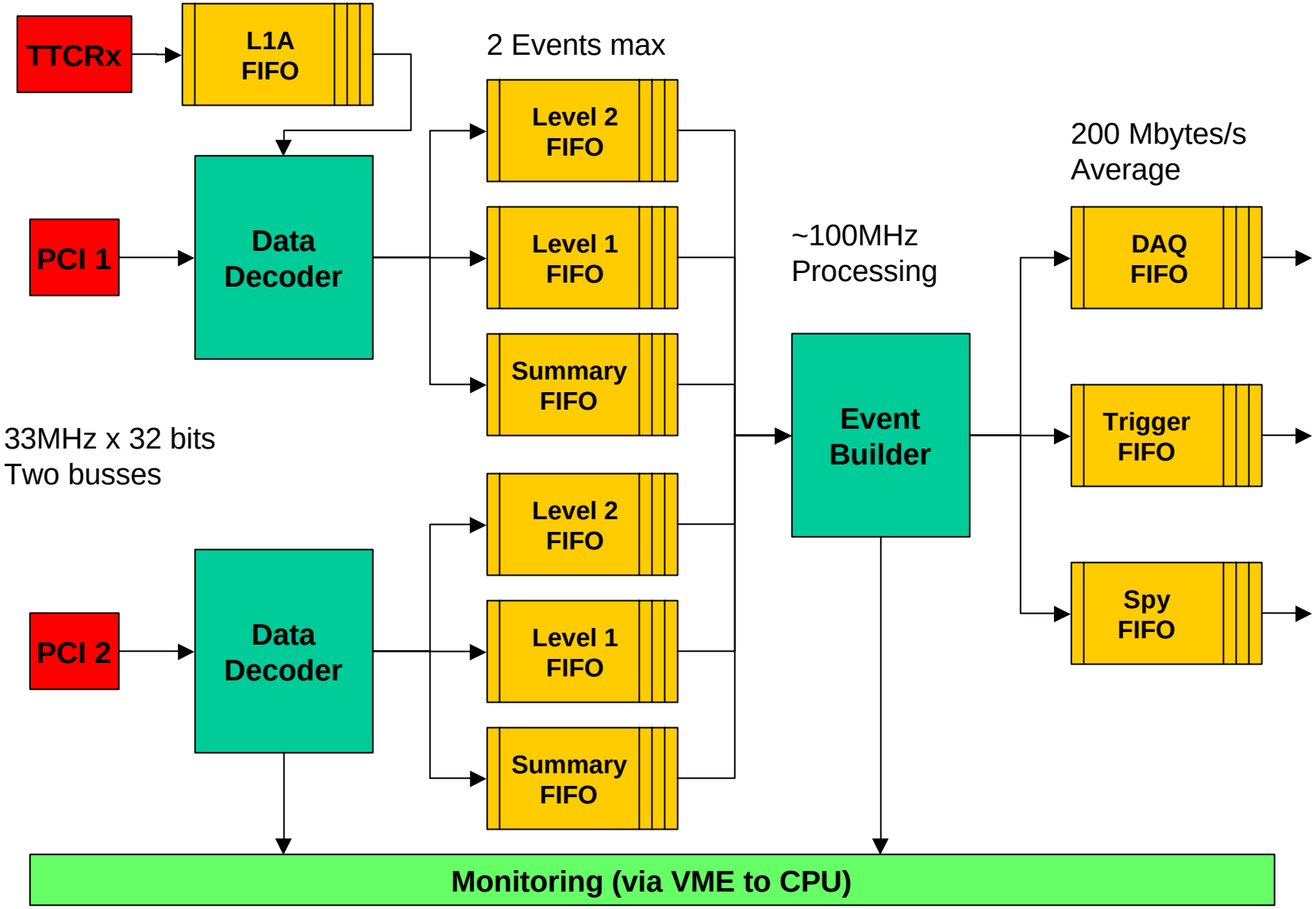

DCC Prototype Logic Board


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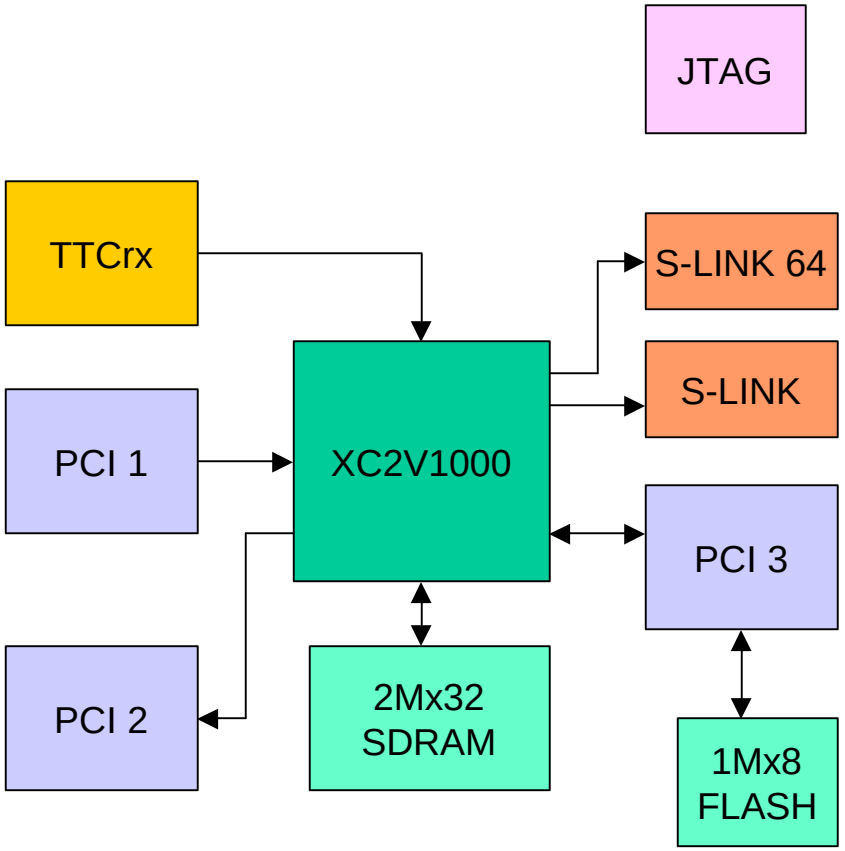
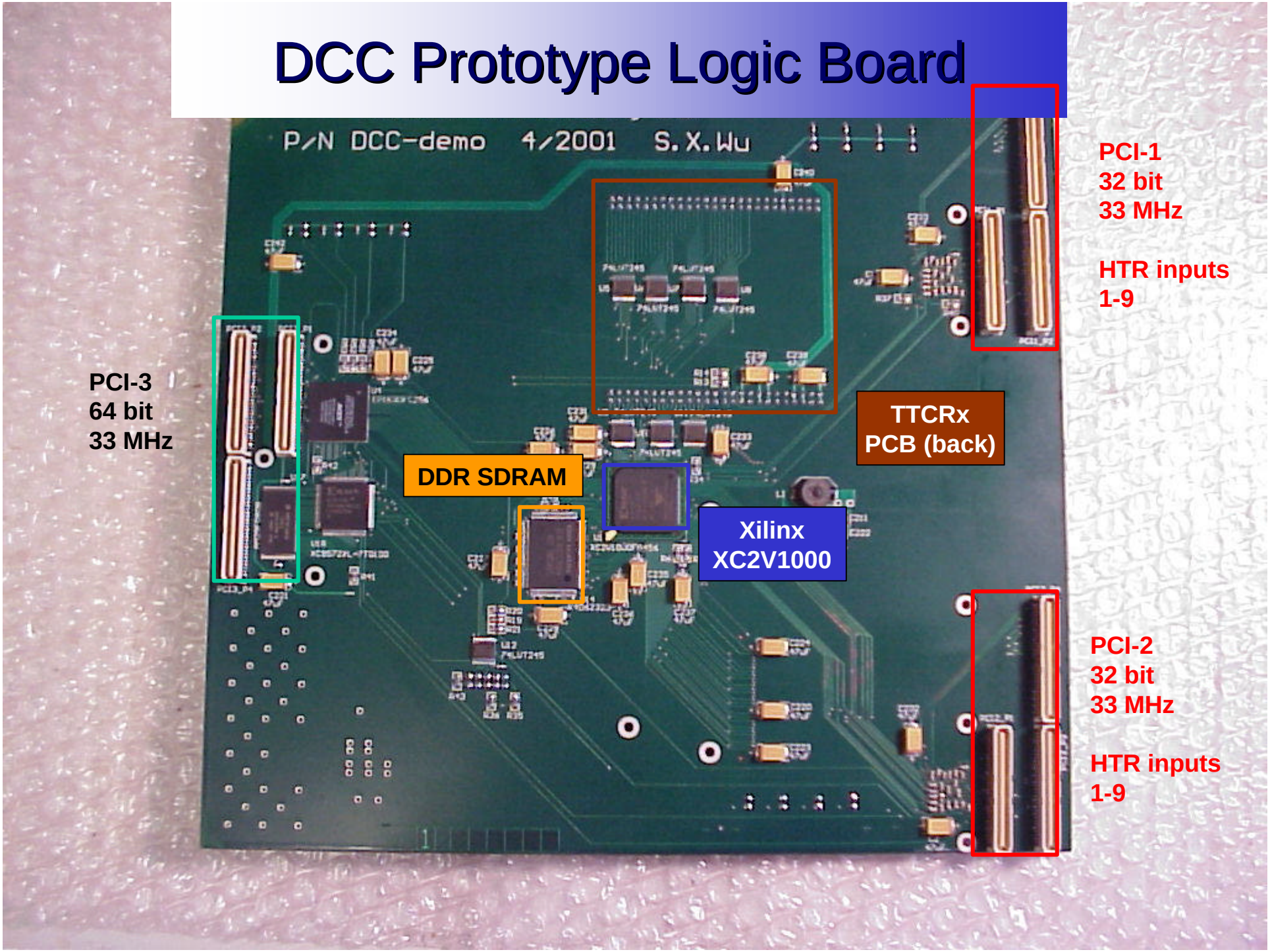
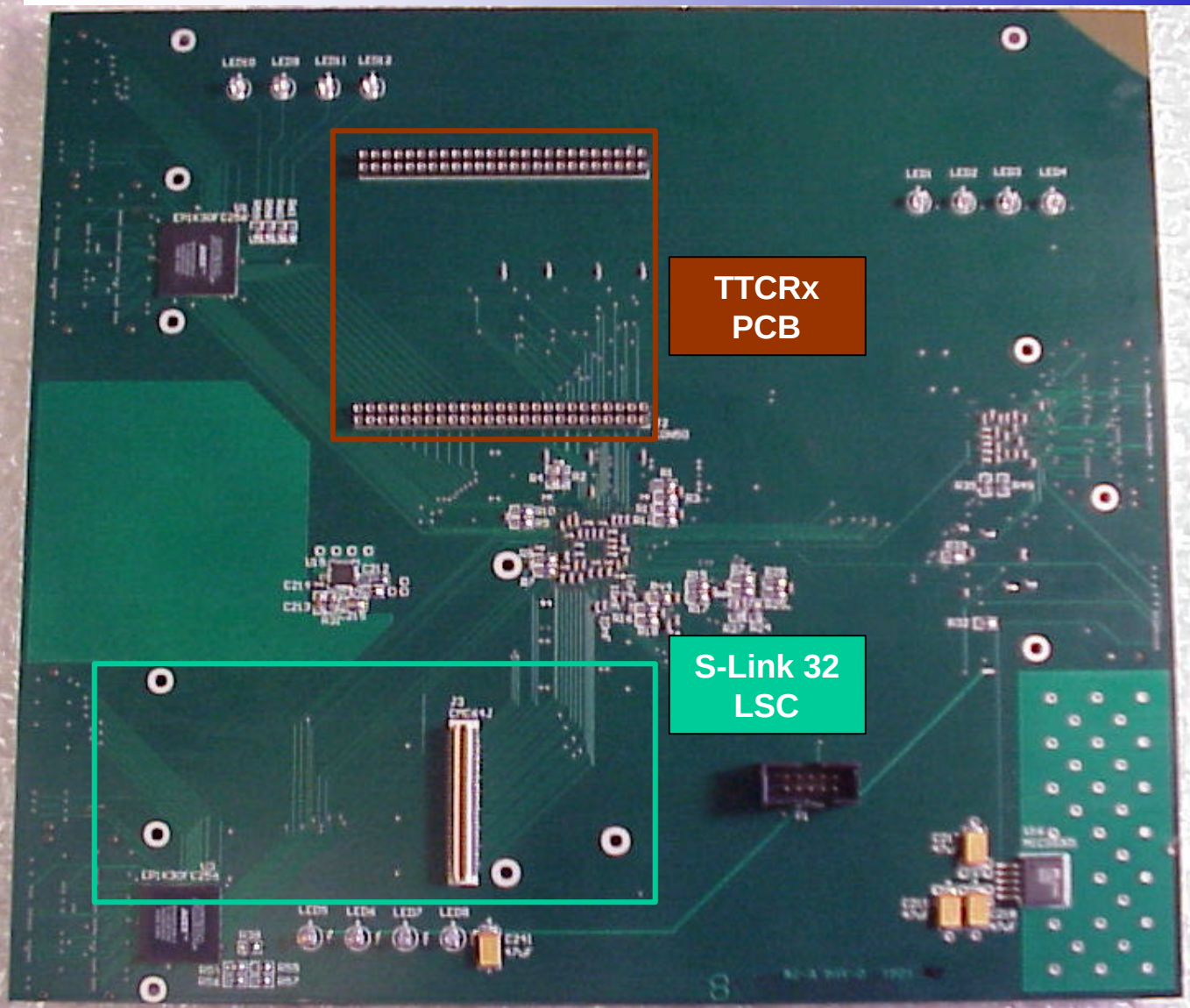
- Features:
  - On-board TTCrx controls operation
  - 3 Altera FPGAs for PCI interfaces (use Altera PCI-MT/32 core)
  - Xilinx Virtex-2 contains all other logic:
    - Event Builder
    - Monitoring
    - Buffering (DDR SDRAM interface at 800Mbytes/s)
    - S-Link output (32 in demo; 64 final)
  - On-board flash memory for FPGA initialization
  - JTAG Interface
- Status:
  - Prototype PCB Working
    - Continuous DAQ transfer at 80MB/s demonstrated (one PCI bus only)
  - 2nd Prototype layout done



DCC Prototype Logic Board



DCC Prototype Logic Board



Data Concentrator Demonstrator

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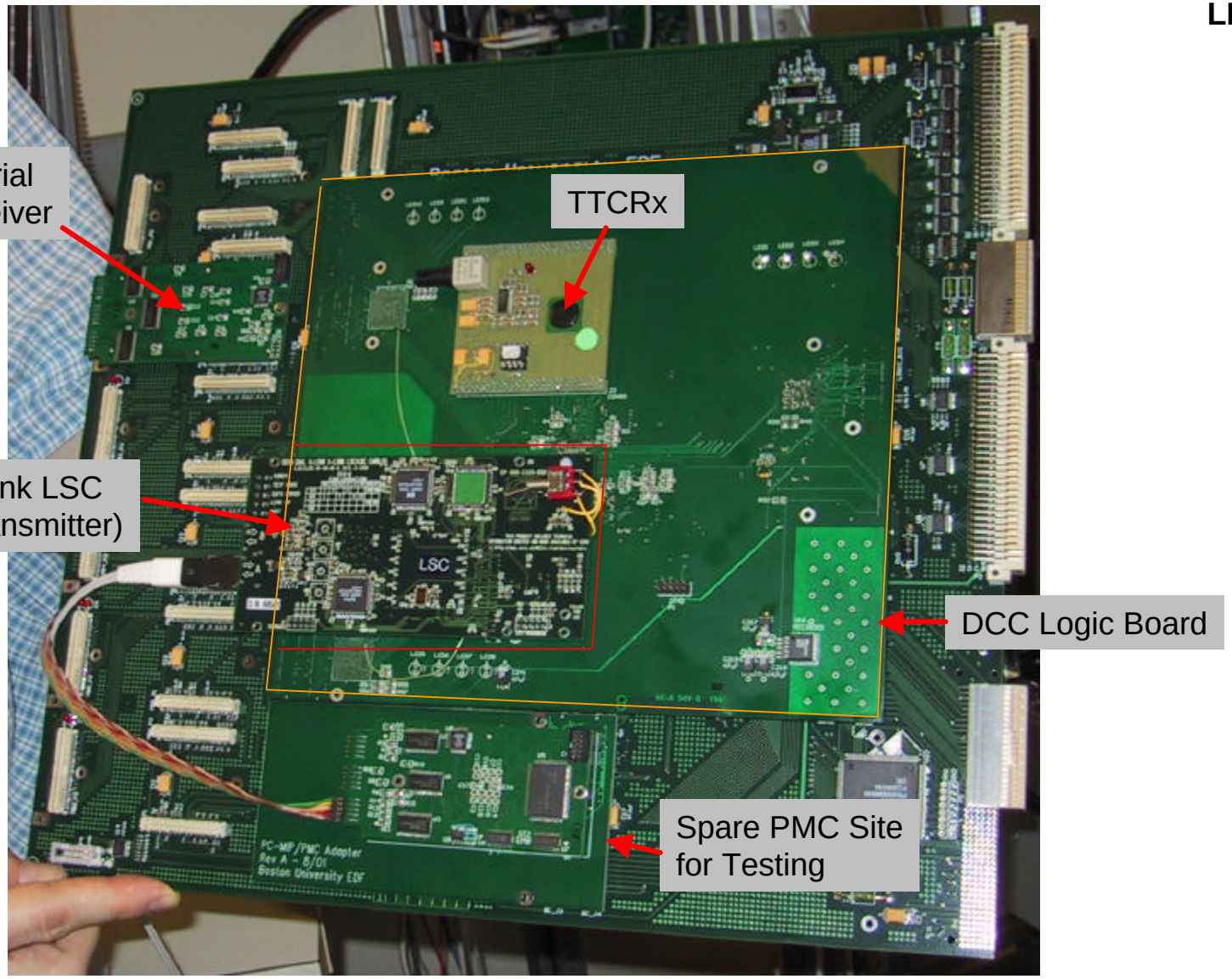
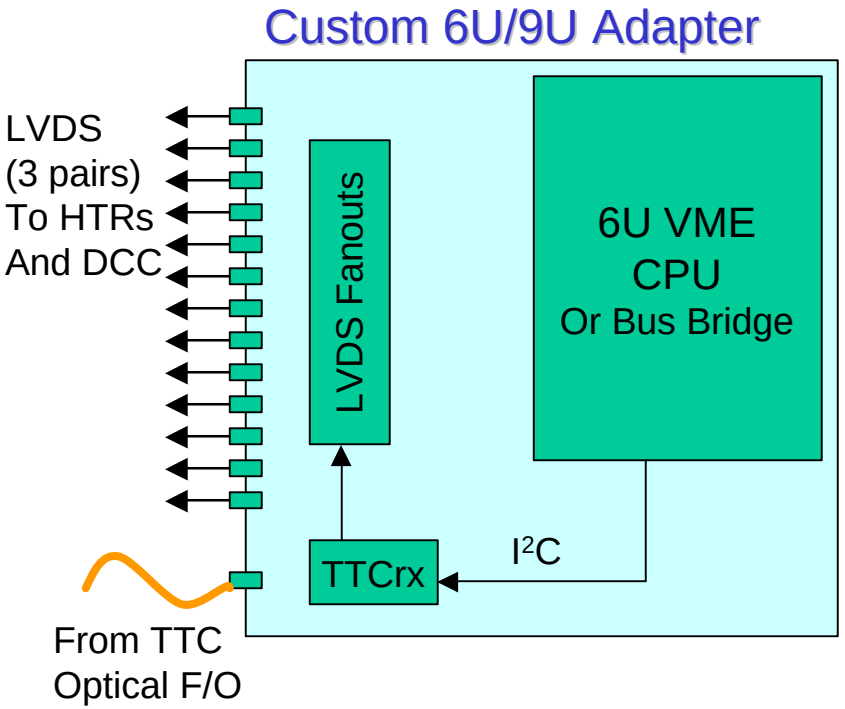


HCAL Readout Controller (HRC)

- Run Control
  - Initialization, shutdown
  - "Slow" monitoring via VME
  - Error recovery:
    - Monitor status registers of modules via VME
    - Report serious errors via DCS
    - Reset/Restart on command
- TTC Fanout
  - Fanout encoded TTC to all modules
  - Fanout Locally Decoded CLK, BC0 to HTR modules
  - I^2C Control of local TTCrx



HCAL DAQ Data Format

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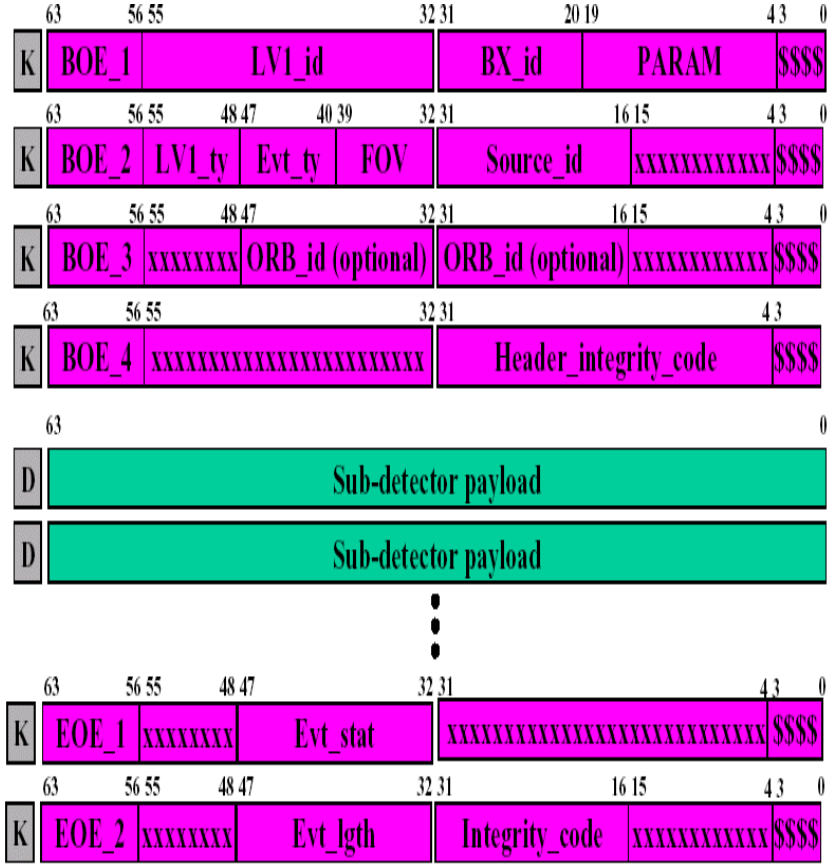
- Data format follows TriDAS Guidelines → → →
- HCAL payload: (details t.b.d)
  - Raw QIE (ADC) samples
  - Level 2 Filter output
  - Trigger Primitives
  - Zero-suppression mask
  - Error summary:
    - Front-end errors
    - Uncorrected Link errors
    - Synchronization errors
- We will stay tuned for updates to the data format → → →



System Tests

- Radioactive Source Calibration Test
  - NOW at Fermilab
  - Record data at 80Mbyte/s for detector calibration
  - Uses demonstrator hardware for all system components and verifies basic functionality
- Test Beam – Summer ’02 at CERN
  - Record data at realistic LHC rates
  - A few hundred channels
  - Uses (2nd) prototype hardware for all components
  - Verify high-rate operation under realistic conditions

Summary

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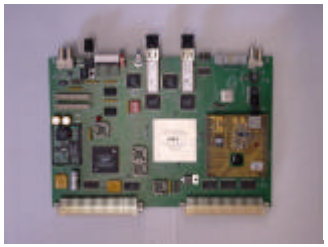
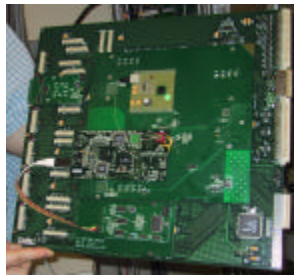
- Front-End:
  - RBX Mechanics/Cooling Designed+Prototyped
  - Readout Card prototypes under test
- HTR:
  - 6U Demonstrator prototypes working
  - New prototype with GOL under design
- DCC:
  - 9U Demonstrator prototypes working
  - No major changes anticipated for production version (significant FPGA coding remains)
- HRC:
  - Use commercial CPU for now
  - TTC Fanout Design Done (U.I.C.)
- Major Concerns:
  - QIE Performance (pending prototype tests now underway)
  - Performance of 1.6 Gbit GOL link
  - HTR/DCC FPGA Design – Quite complex

HCAL RBX

HTR Demonstrator



DCC Demonstrator



VME Pentium CPU

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Backup Slides

HCAL DAQ Buffering

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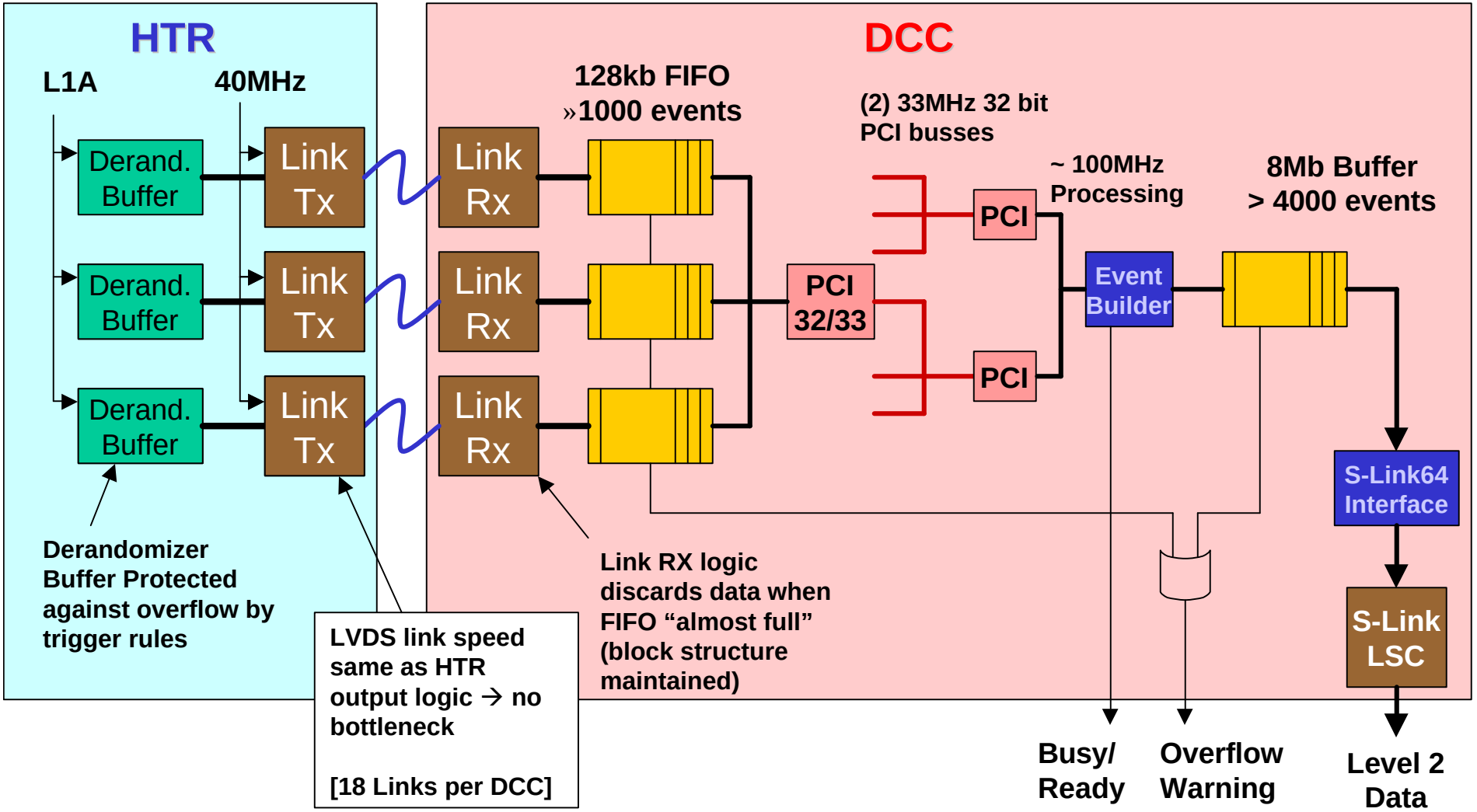
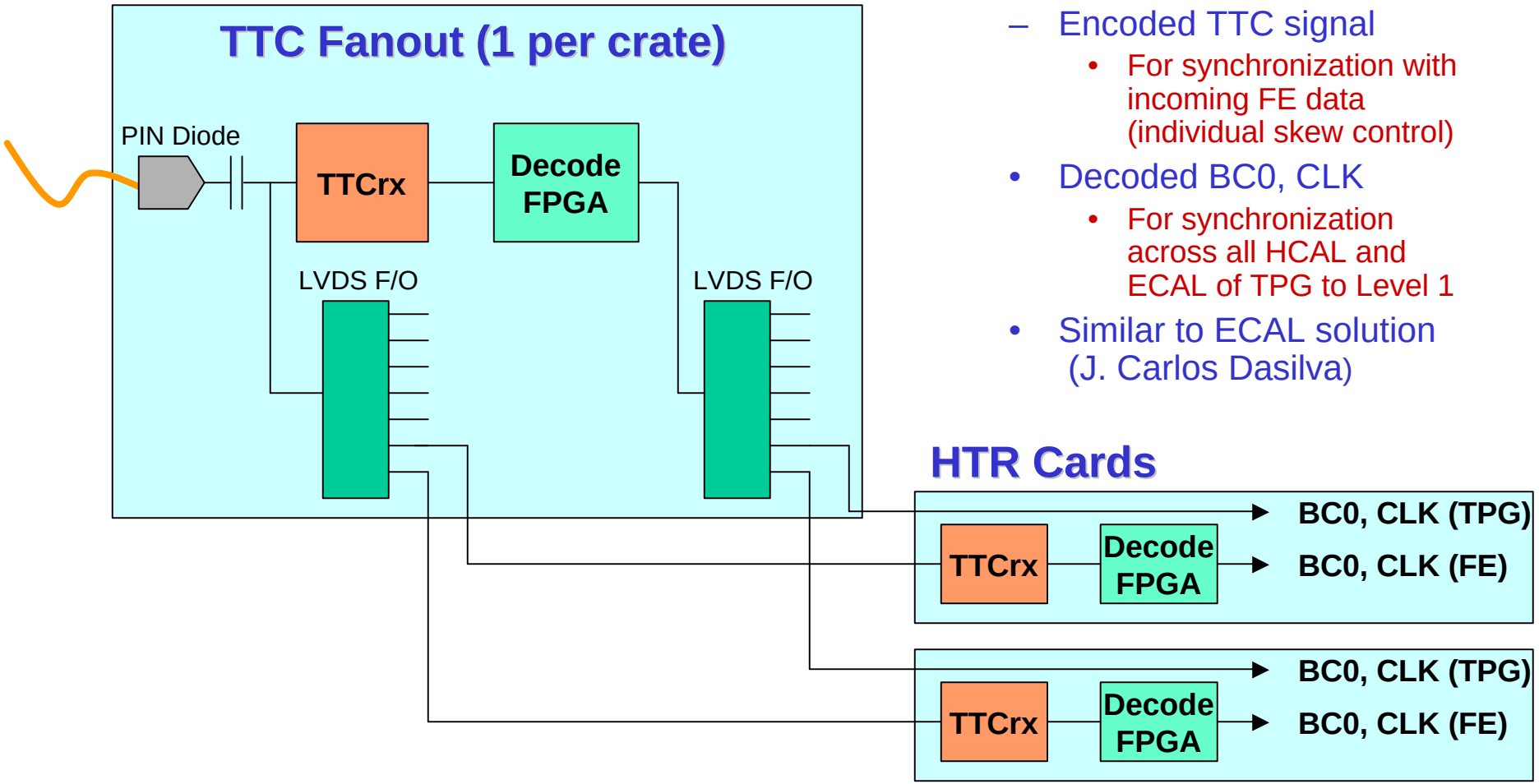


HCAL Timing / L1A Distribution

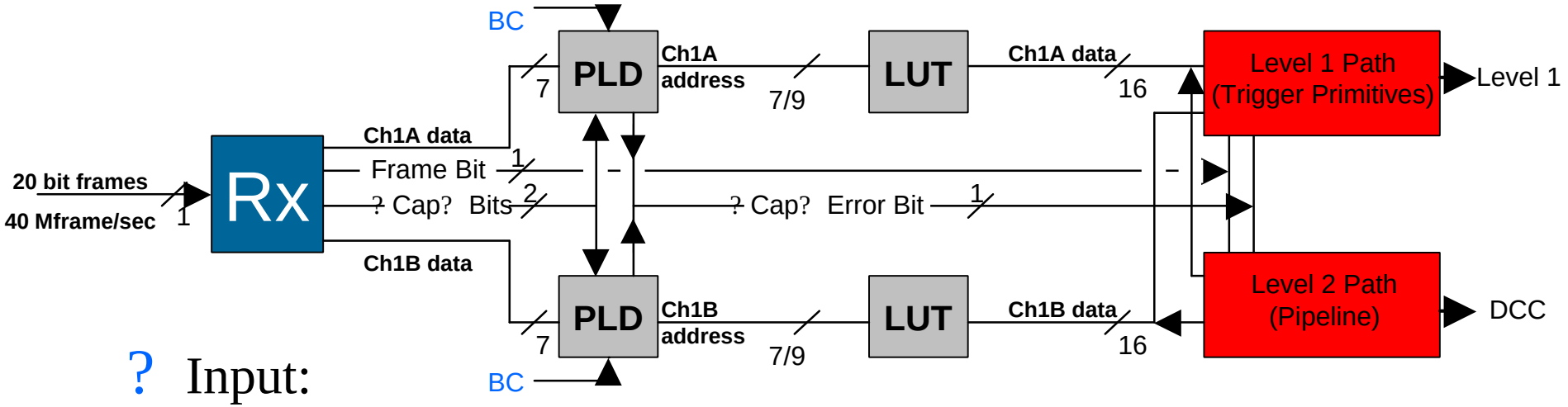
- Fanout Both:
  - Encoded TTC signal
    - For synchronization with incoming FE data (individual skew control)
  - Decoded BC0, CLK
    - For synchronization across all HCAL and ECAL of TPG to Level 1
  - Similar to ECAL solution (J. Carlos Dasilva)



HCAL Controls and Monitoring

- Fast Controls (via TTC):
  - L1A, Start Run, Stop Run
  - Reset (complete and partial – need to define!)
- Fast Monitoring (dedicated signals to TTS)
  - Overflow Warning (buffer full above preset limit)
  - Busy/Ready (reset, start/stop completed)
- Slow Monitoring (link errors, loss of sync, etc)
  - Counters in FPGAs collect information in real time
  - Reported via CPU

HTR Details

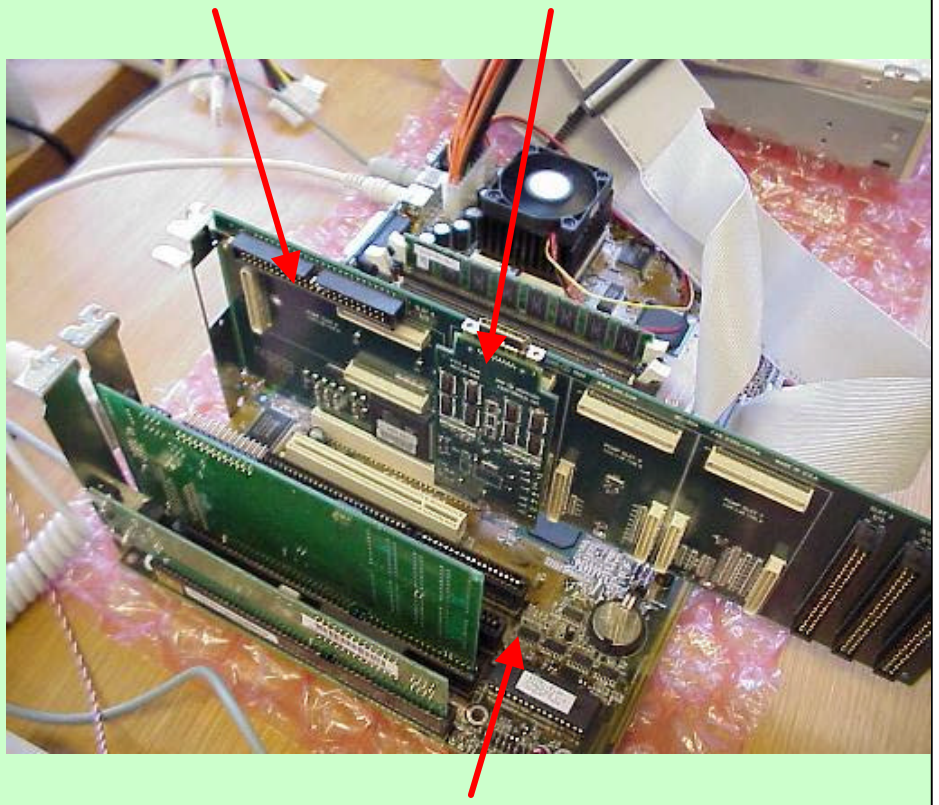


- Input:
  - QIE 7 bit floating plus 2 bits ? cap?
- Lookup table (LUT)
  - Convert to 16 bit linear energy
- Pipeline (? Level 1 Path?)
  - Transmit to Level 1 trigger, buffer for Level 1 Accept, 3 μs latency
- Level 2 Buffer (? Level 2 Path?)
  - Asynchronous buffer, sized based on physics requirements

PCI Development

- PC-MIP Cards
  - Use adapter in standard PC motherboard
  - LRB Prototype was completely developed before motherboard
- VME Motherboard
  - Test all sites with standard PC-MIP and PMC cards
- Integration
  - Integration of motherboard and mezzanine cards was quite smooth
- PCI Interface logic
  - Use Altera Core (motherboard and logic boards)
  - Own design simple slave for LRB

PCI Test Setup



Flash ADC Quantization

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