# Data Concentrator Card for ECAL

- **Presentation Outline**
  - **ECAL Data Volume and Raw Data generation**
  - **DCC Conceptual Design**
  - **Modeling and Simulation of the Hardware**

# DCC TEAM

## DCC Requirements

João Varela

## ECAL Raw Data Simulation

Nuno Almeida

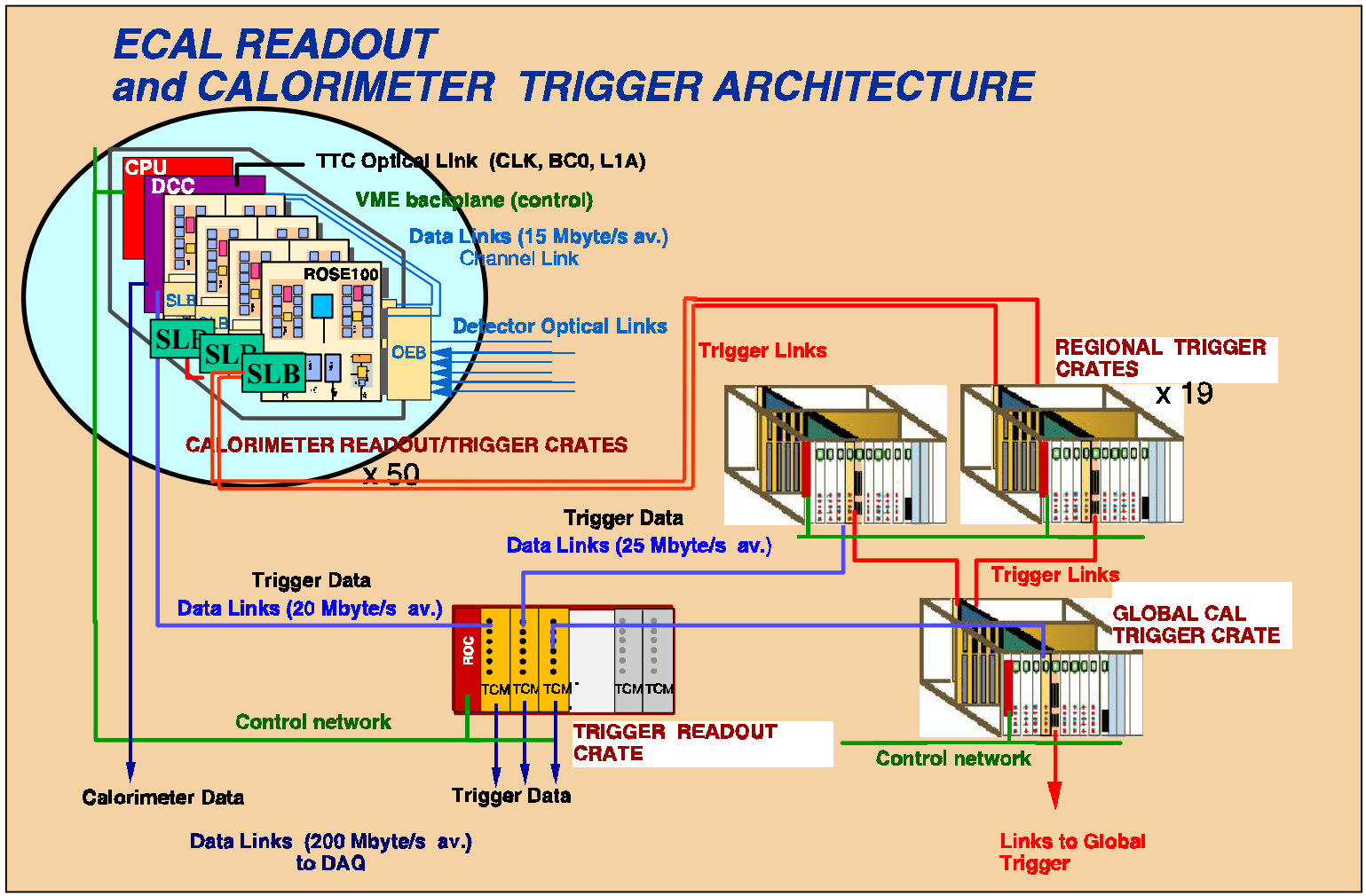
## Modelling and Hardware Simulation

António Correia, Pedro Machado, Pedro Moura, Vasco Bexiga, Isabel Teixeira

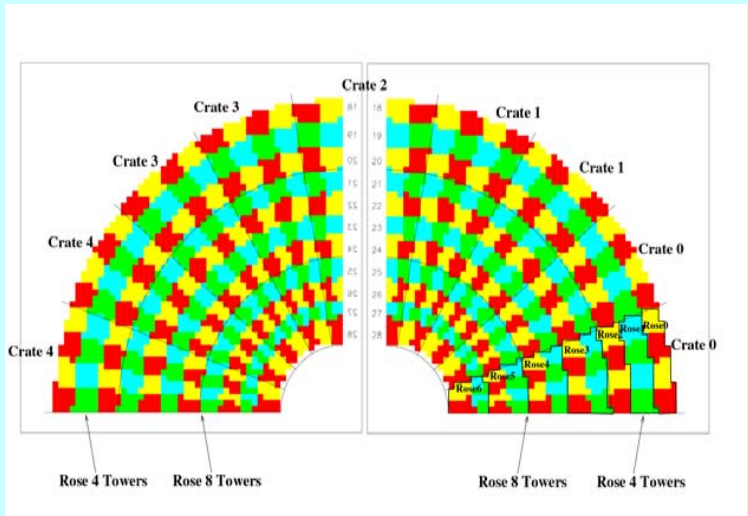
## DCC Design and Conception

José C. Da Silva

# ECAL Readout Architecture



# ECAL Geometry and Readout Hardware

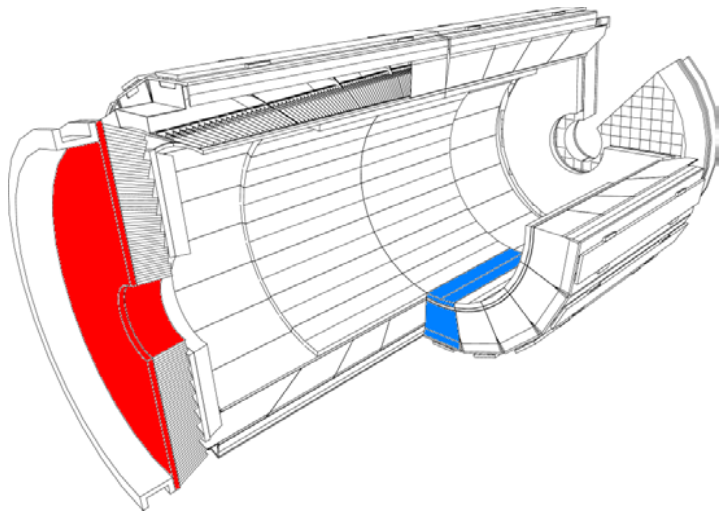


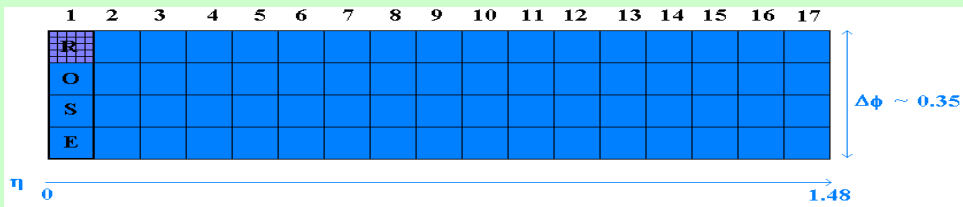

## ENDCAPS :

Each trigger Tower will have a variable number of crystals. In order to optimize links capabilities, each ROSE board will handle a variable number of Trigger Towers (4,6 or 8)

Due to electronic tests and geometric constraints, there are 2 kinds of DCC, handling 7 (DCC1) or 14 (DCC2) ROSE modules

In the endcaps there will be in total 20 DCC : 16 DCC1 and 4 DCC2.






## BARREL :

Each ROSE handles 4 consecutive Trigger Towers in phi (100 crystals).

Each DCC handles 17 consecutive ROSE modules in eta what corresponds to one Supermodule , or one ECAL Crate.

There will be 36 DCC modules (18 per half-barrel)

# Raw Data Simulation Conditions

- **Signal input: jets 50<pt<100 GeV, at high luminosity (L~$10^{34}$/$cm^2$/s ) corresponding to ~17 pileup events/crossing**

- **Full ECAL Detector Simulation was performed using ORCA (Object Oriented Reconstruction for CMS Analysis) version 4_4_0_optimized.**

- **ECAL raw data was simulated with an additional developed File Data Package**

- **Simulation of ECAL Data Volumes was performed for various scenarios of zero suppression and tower selective readout.**

# ECAL Selective Readout

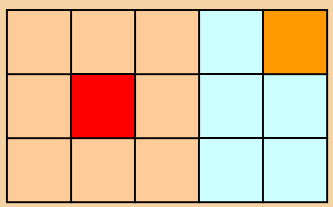
•Target Data Volumes tranfered to DAQ are 1MB for the total data event, being 100 KB reserved to ECAL (~2KB per DCC). Full ECAL data readout imply an ECAL data volume of 1.86MB per triggered event.

•Selective Readout tecniques must be applied to achieve a reduction factor of ~20 in ECAL data:

Zero Supression

Supression of crystals with energy lower than 2σ
~ 60MeV (Barrel) and ~ 300 Mev(EndCaps)

Tower Selective Readout

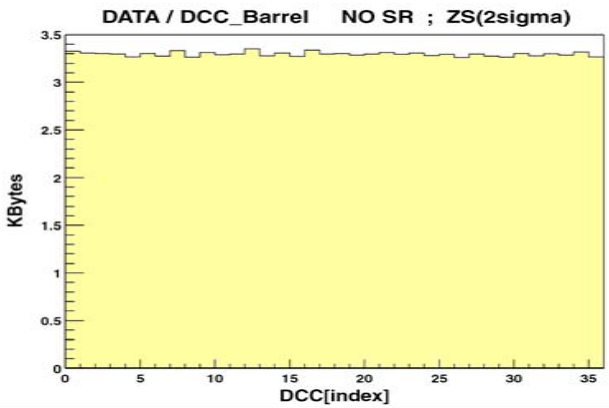


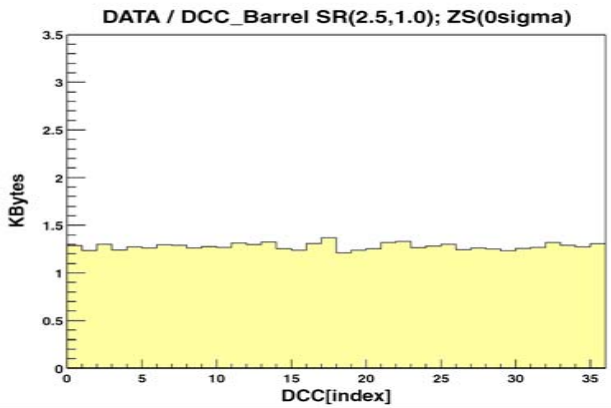
CENTER ⟹ $Et > H_{TH}$
SINGLE ⟹ $H_{TH} > Et > L_{TH}$
NEIGHBOUR ⟹ $Et < L_{TH}$
NOTREAD ⟹ $Et < L_{TH}$
and not neighbour....

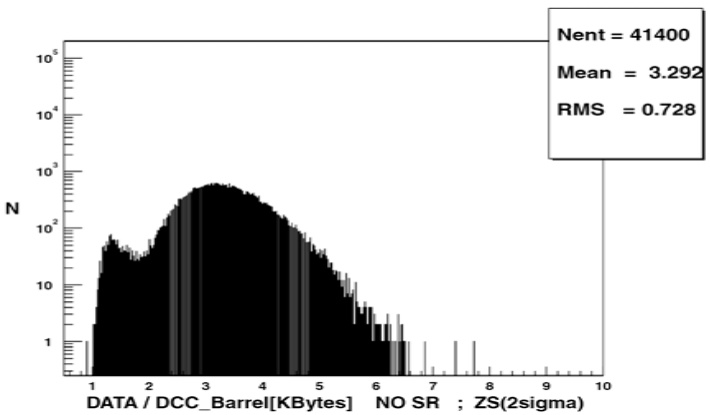
$H_{TH}$ ~ 2.5 GeV

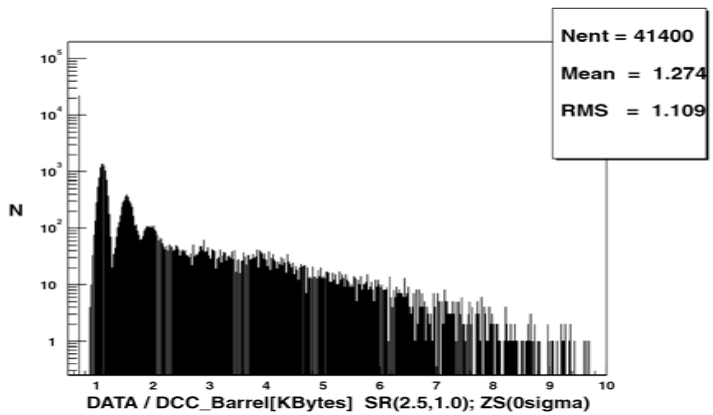
$L_{TH}$ ~ 1.0 GeV

# Barrel DCC Event Size

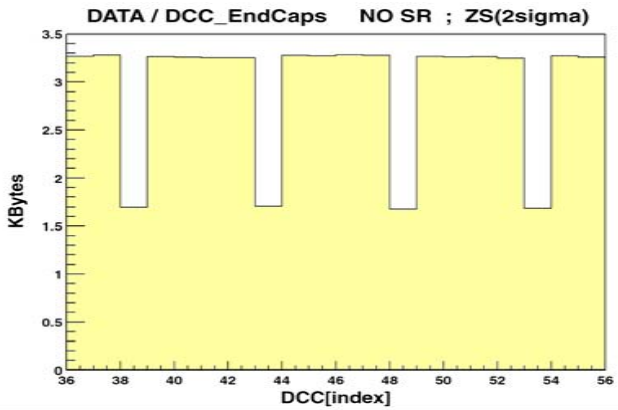


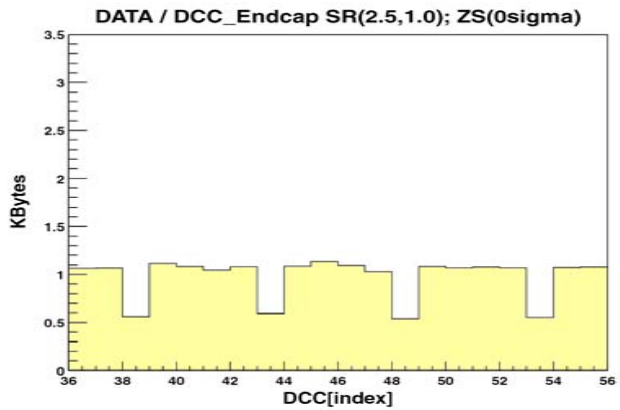



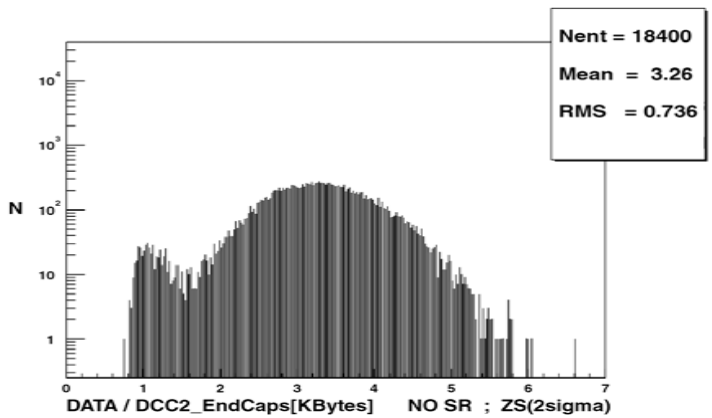



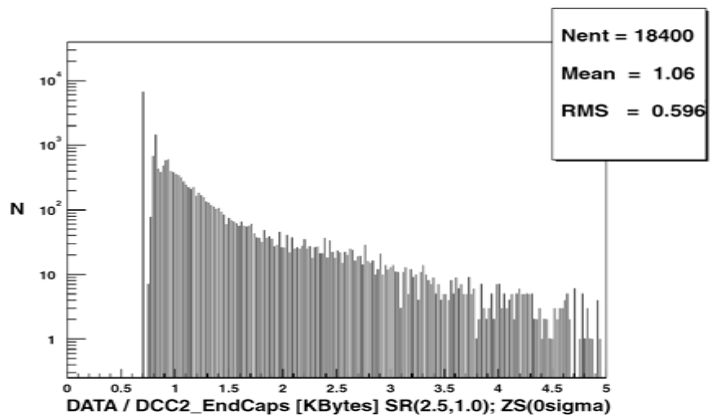



# Endcap DCC Event Size



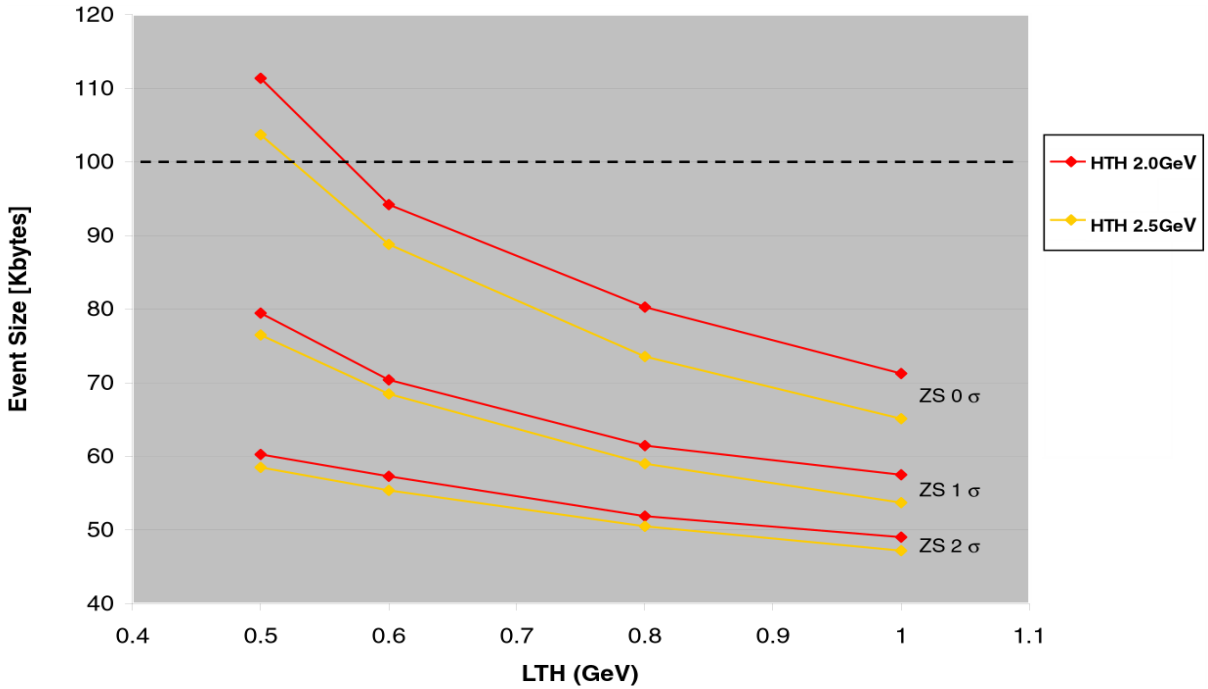




**ECAL EventSize = 177.49 Kb** **ECAL EventSize = 65.42 Kb**

# ZS & SR Scenarios



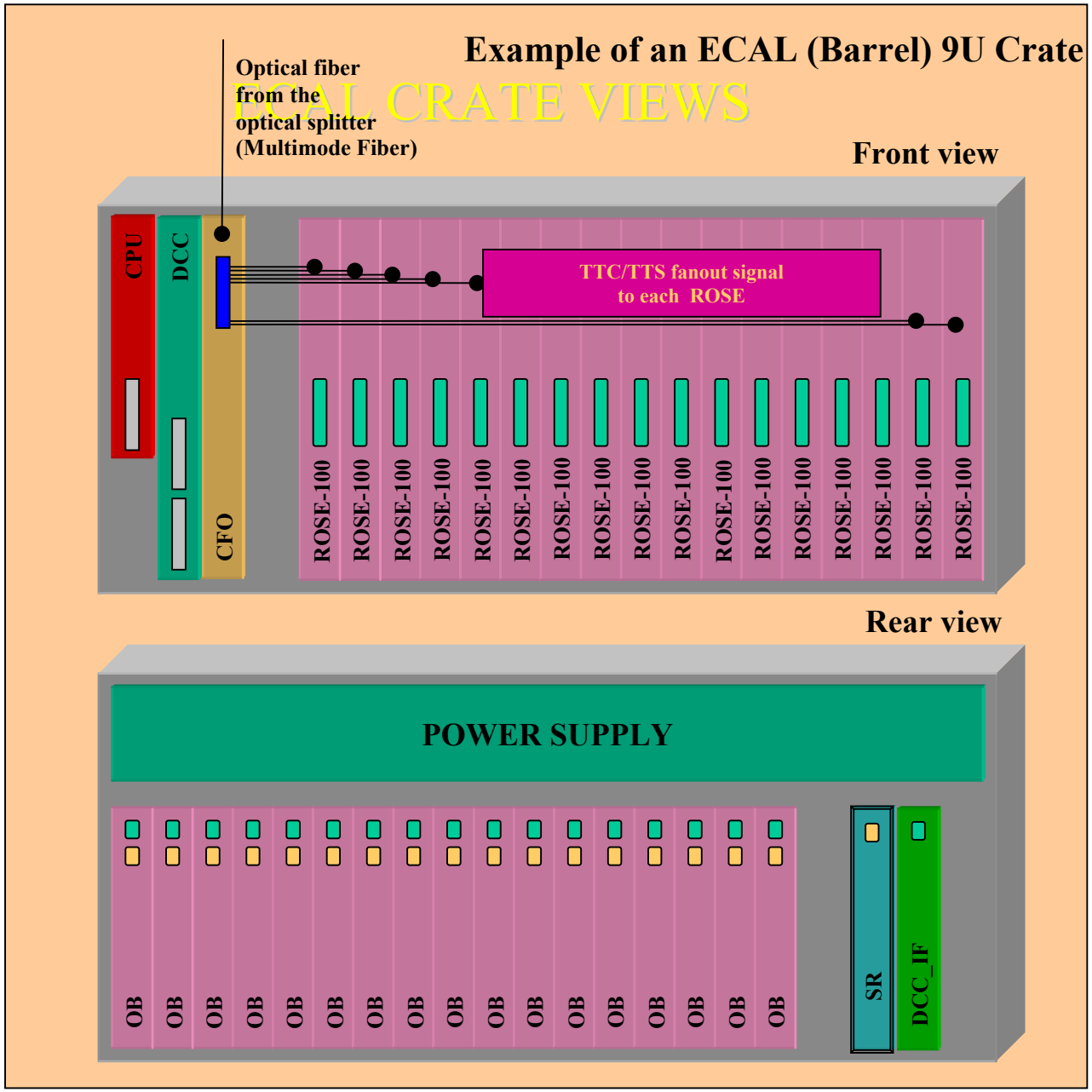

- **Tower Selective Readout thresholds selection must depend on the ZS applied : Setting Hth = 2.0 GeV, Lth = 0.6 GeV with ZS at 0σ we obtain an average ECAL Event Size of 95 Kb without losing significant physics data and obeying ECAL data volume target of 100Kb .**

# Data Concentrator Card for ECAL

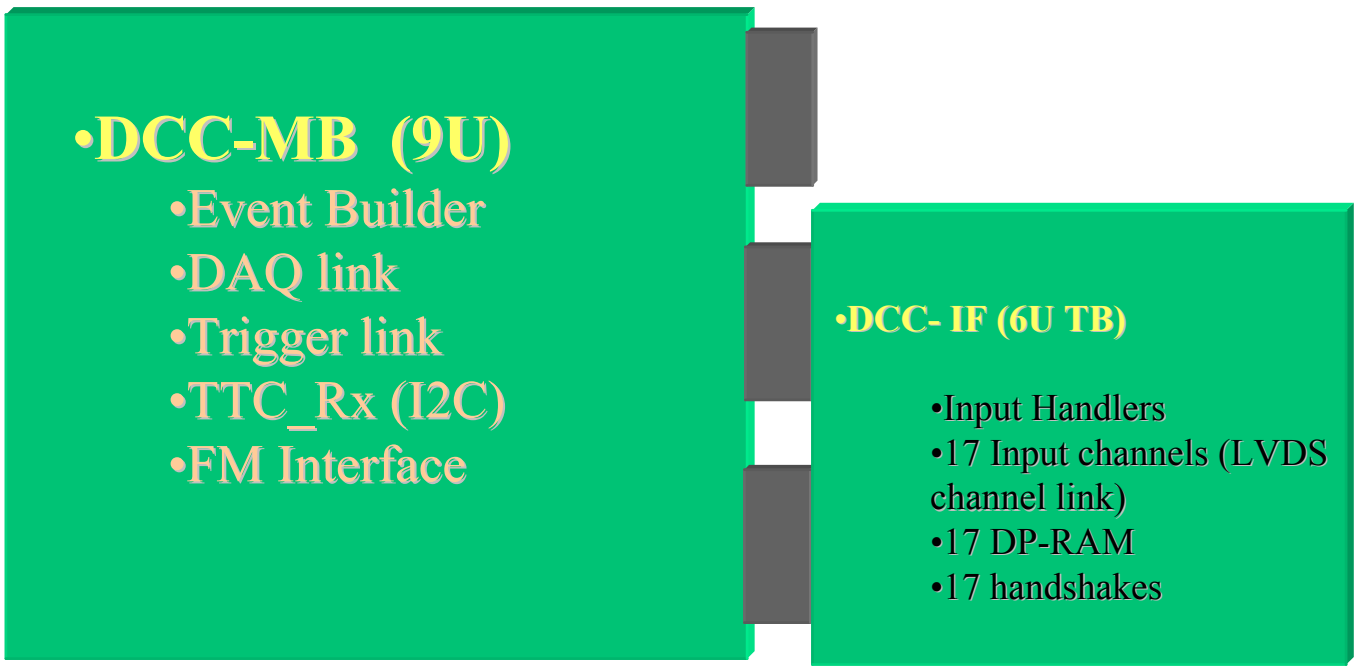
- **DCC Conceptual Design**



José C. Da Silva


Example of an ECAL (Barrel) 9U Crate
ECAL CRATE VIEWS
Optical fiber
from the
optical splitter
(Multimode Fiber)
Front view
CPU
DCC
CFO
TTC/TTS fanout signal
to each ROSE
ROSE-100
Rear view
POWER SUPPLY
OB
SR
DCC_IF

# ECAL DCC partition

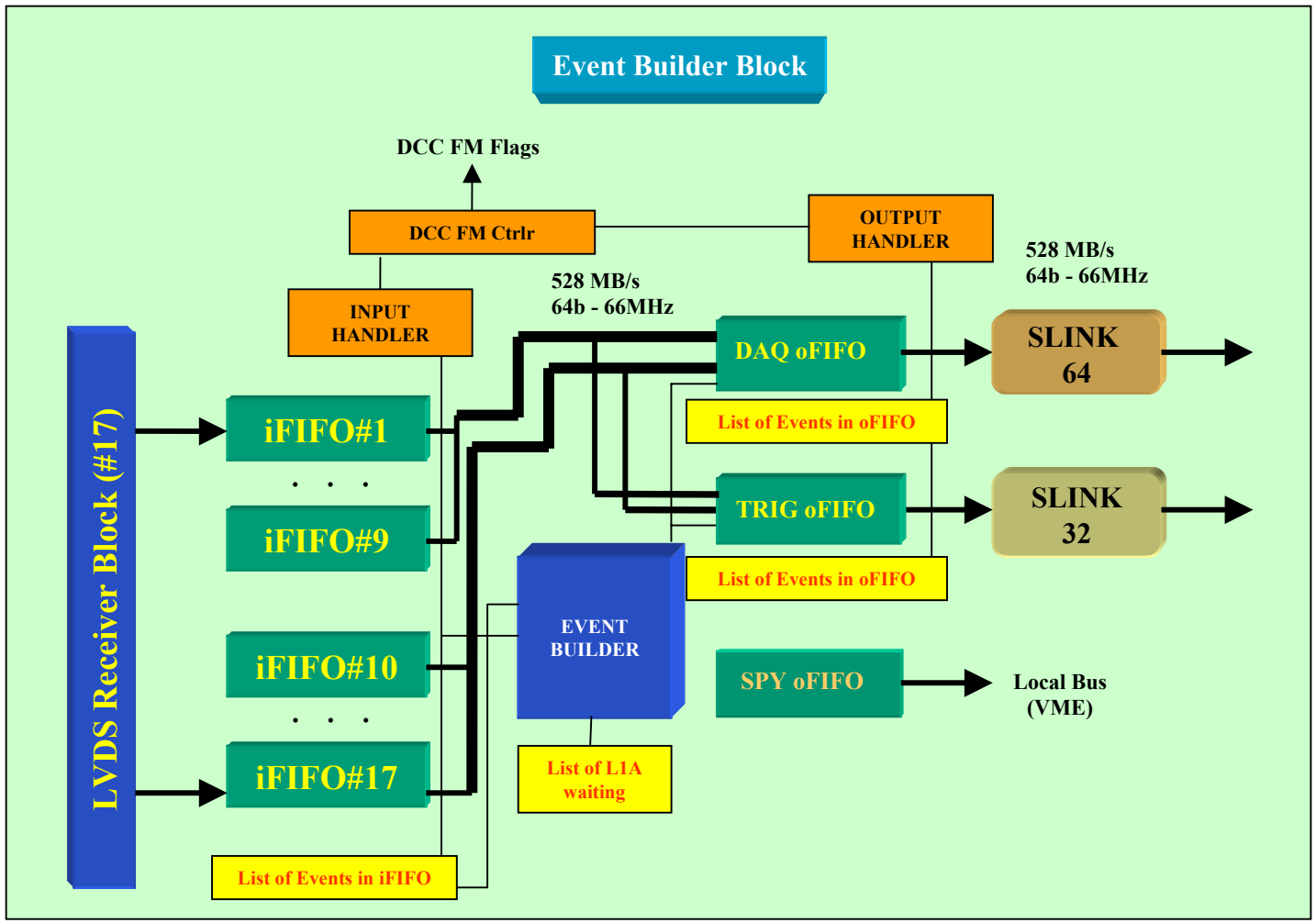



•DCC (2 Boards)

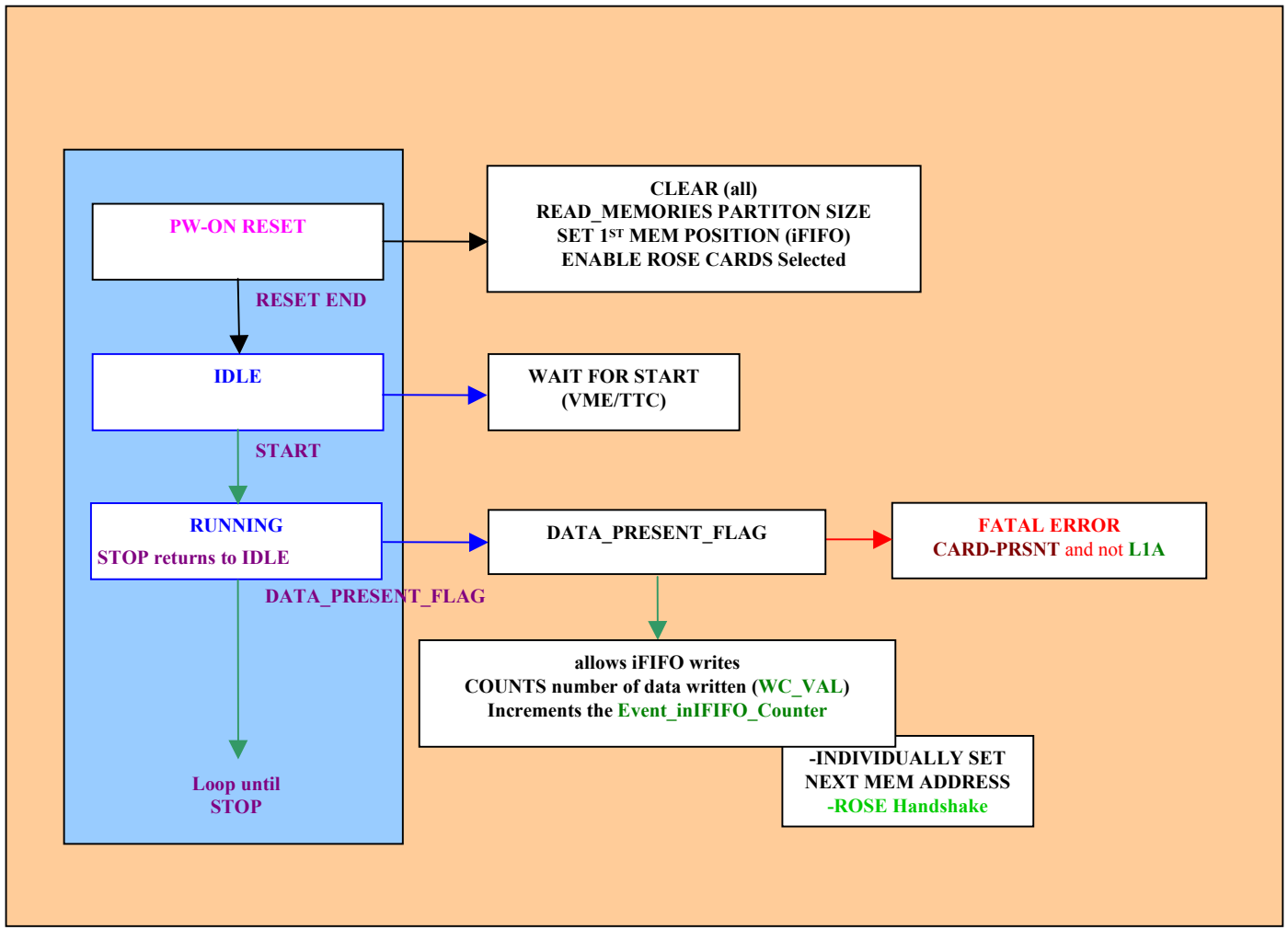
# DCC Technological Choices

- **17 LVDS Channel Link inputs**
  - **32 Bits @ 40MHz**
  - **Input channel masking**
- **Input Dual Port Memories (32k x 36 bit - 66Mhz)**
  - **pre programmed partition size**
- **Internal Event Builder**
  - **Dual Internal Bus (Bandwidth up to 528MB/s)**
- **Outputs**
  - **Data Transfer to the ECAL DAQ (SLINK 64) and Trigger DAQ (SLINK 32)**
  - **Event Spy memory (VME)**

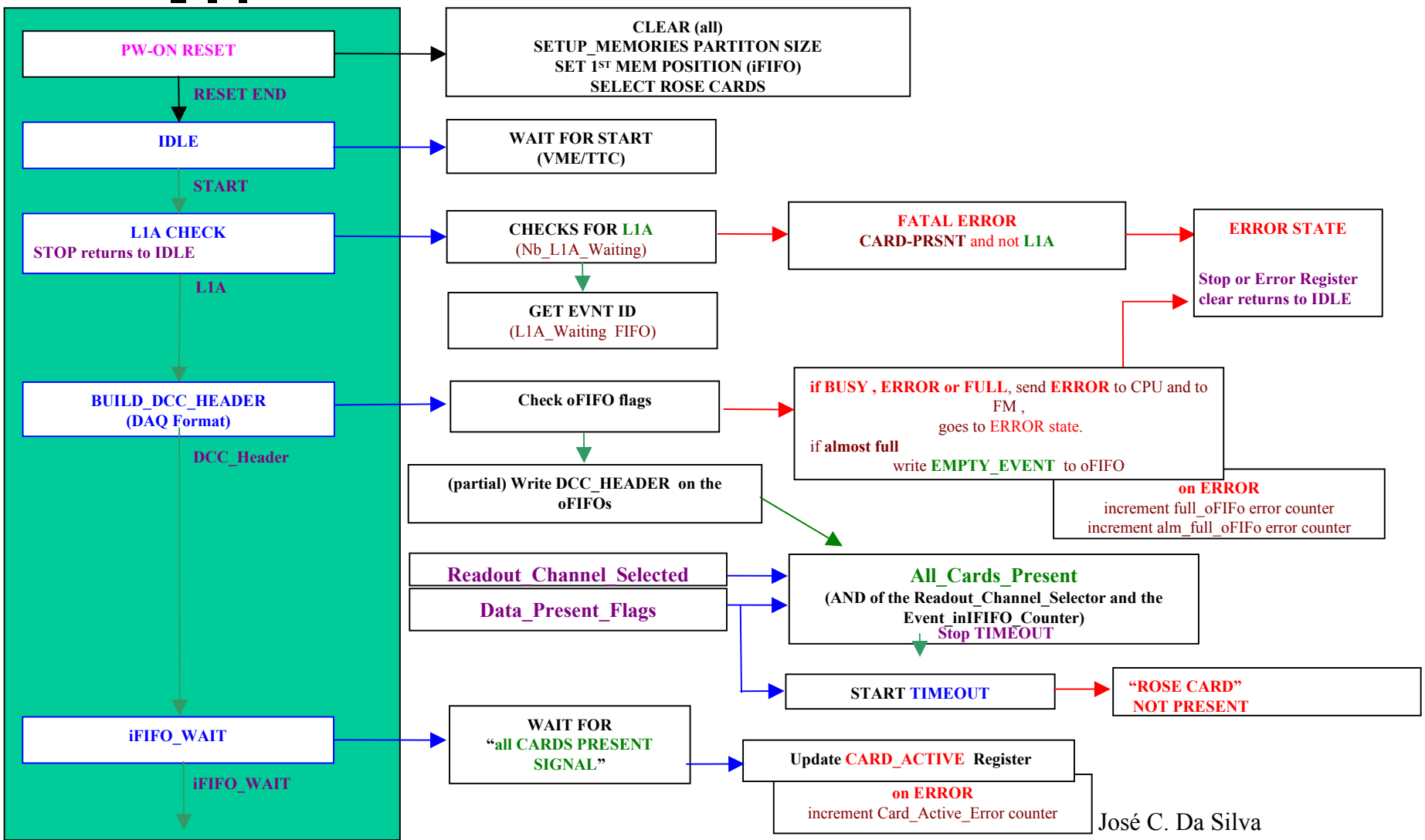
# EVENT BUILDER BLOCK DIAGRAM



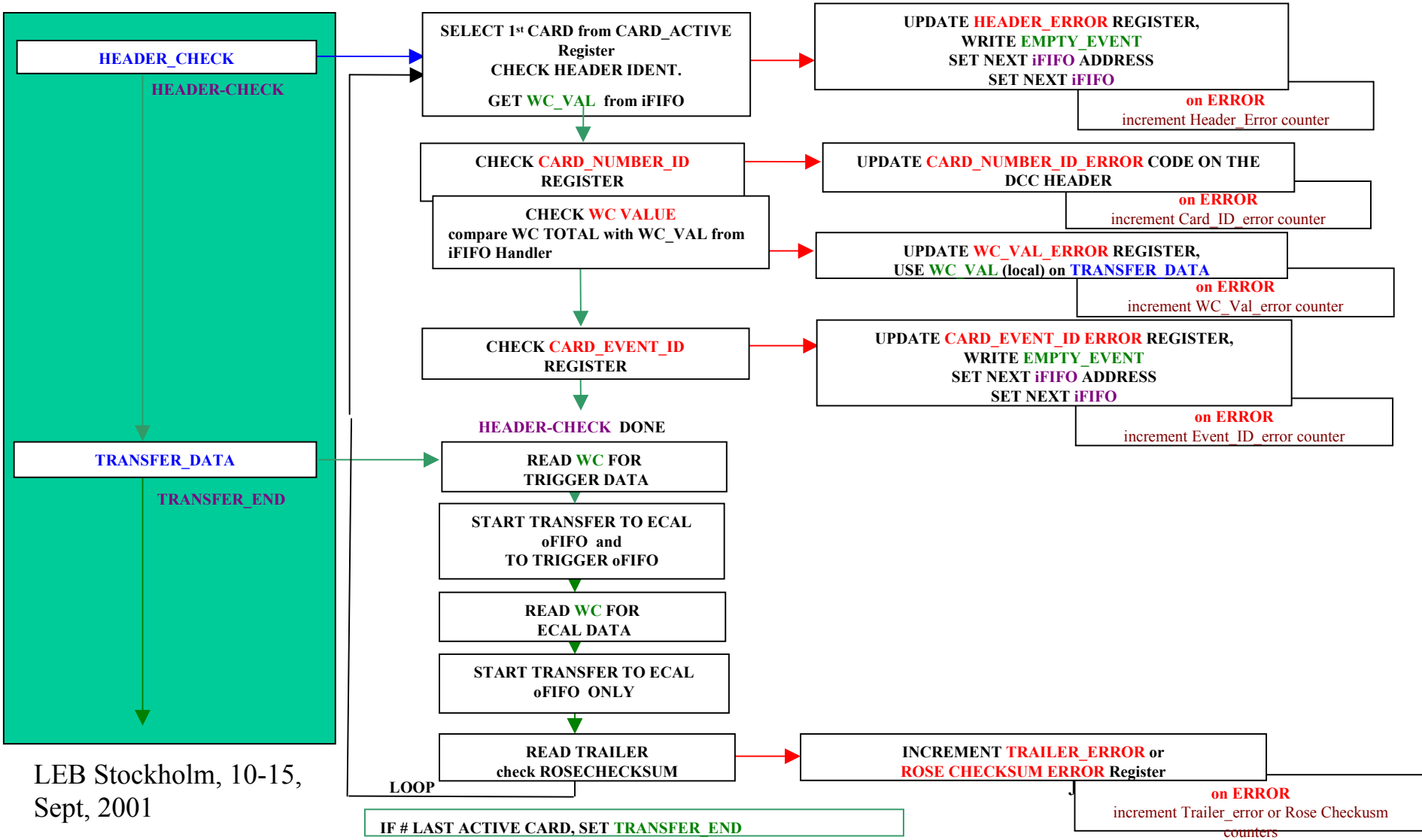
# Input Handler



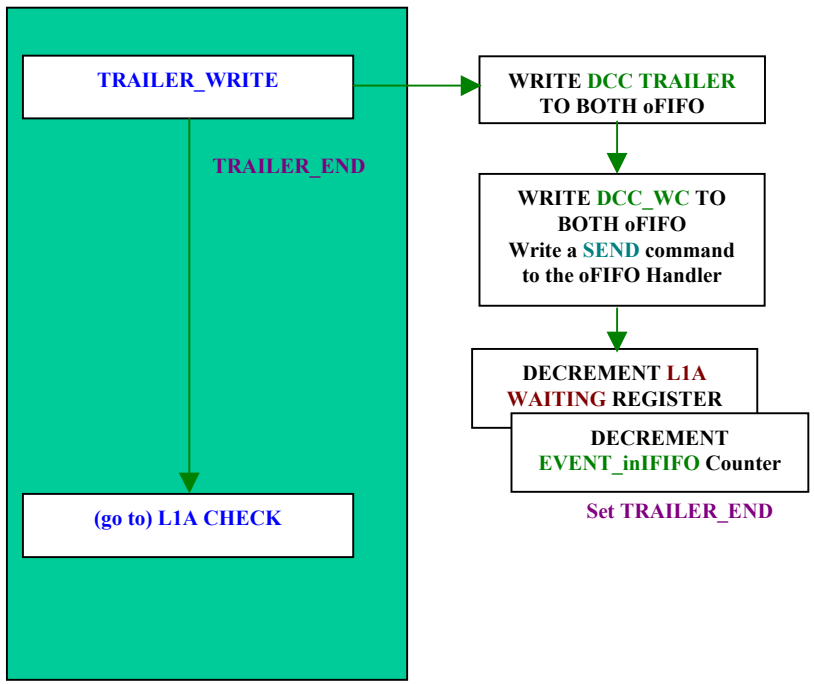
# Event Builder SM (1)



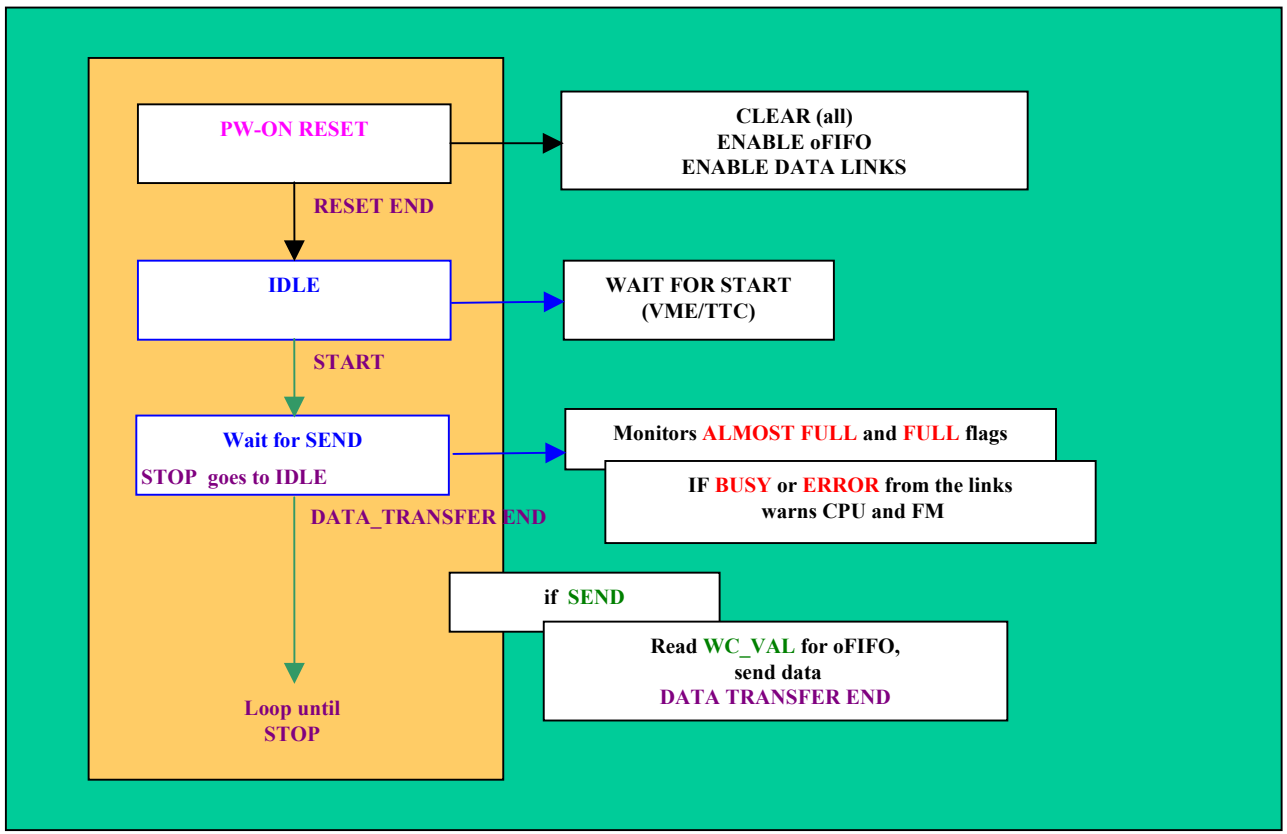
# Event Builder SM (2)



# Event Builder SM (3)



# Output Handler

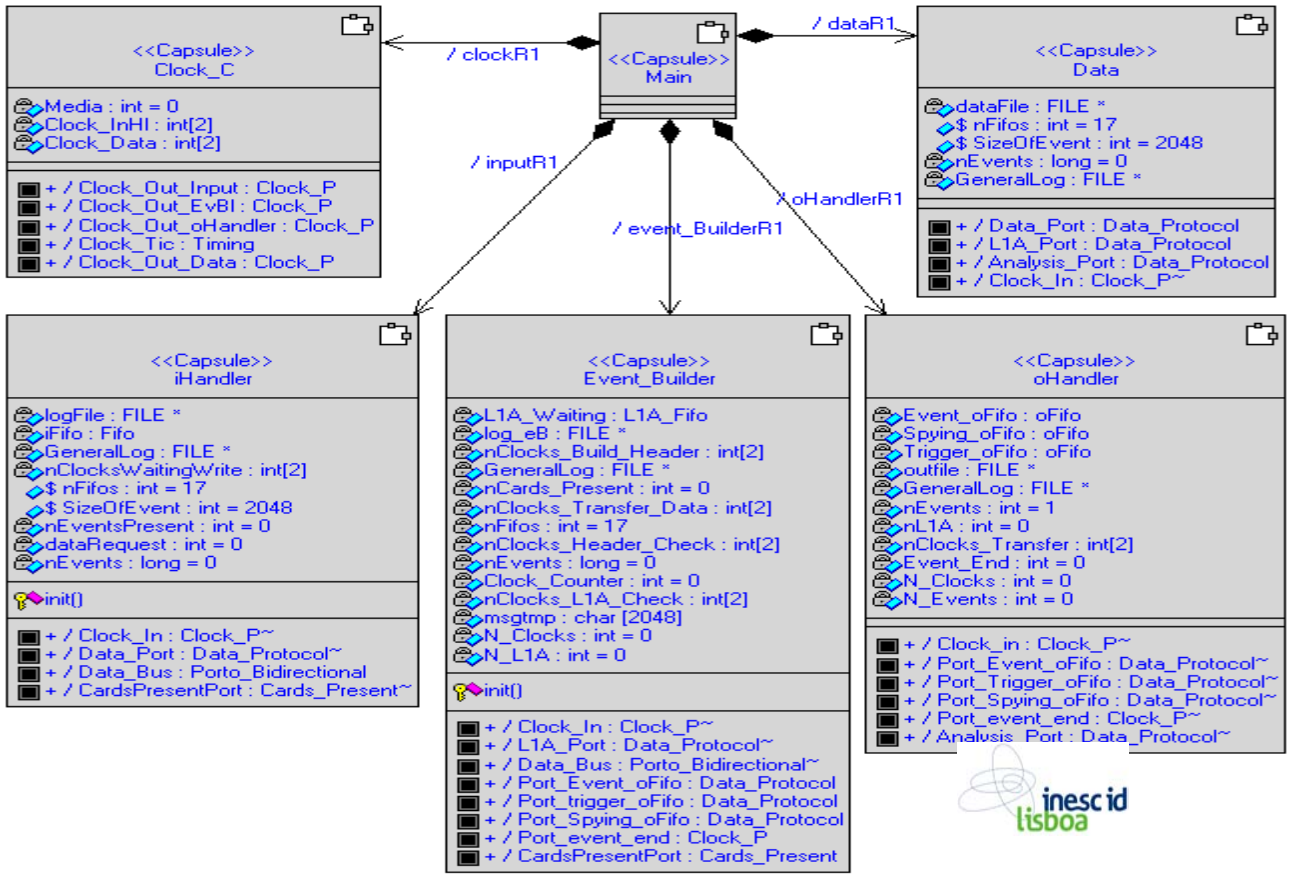


# Hardware Modeling and Simulation

- **Raw data simulated with ORCA used as input**
- **Modeling of the Hardware**
- **Preliminary results of DCC simulation**

# Hardware Modeling

- System Simulation using Rational Rose Real Time
- Input Raw Data from ORCA simulation

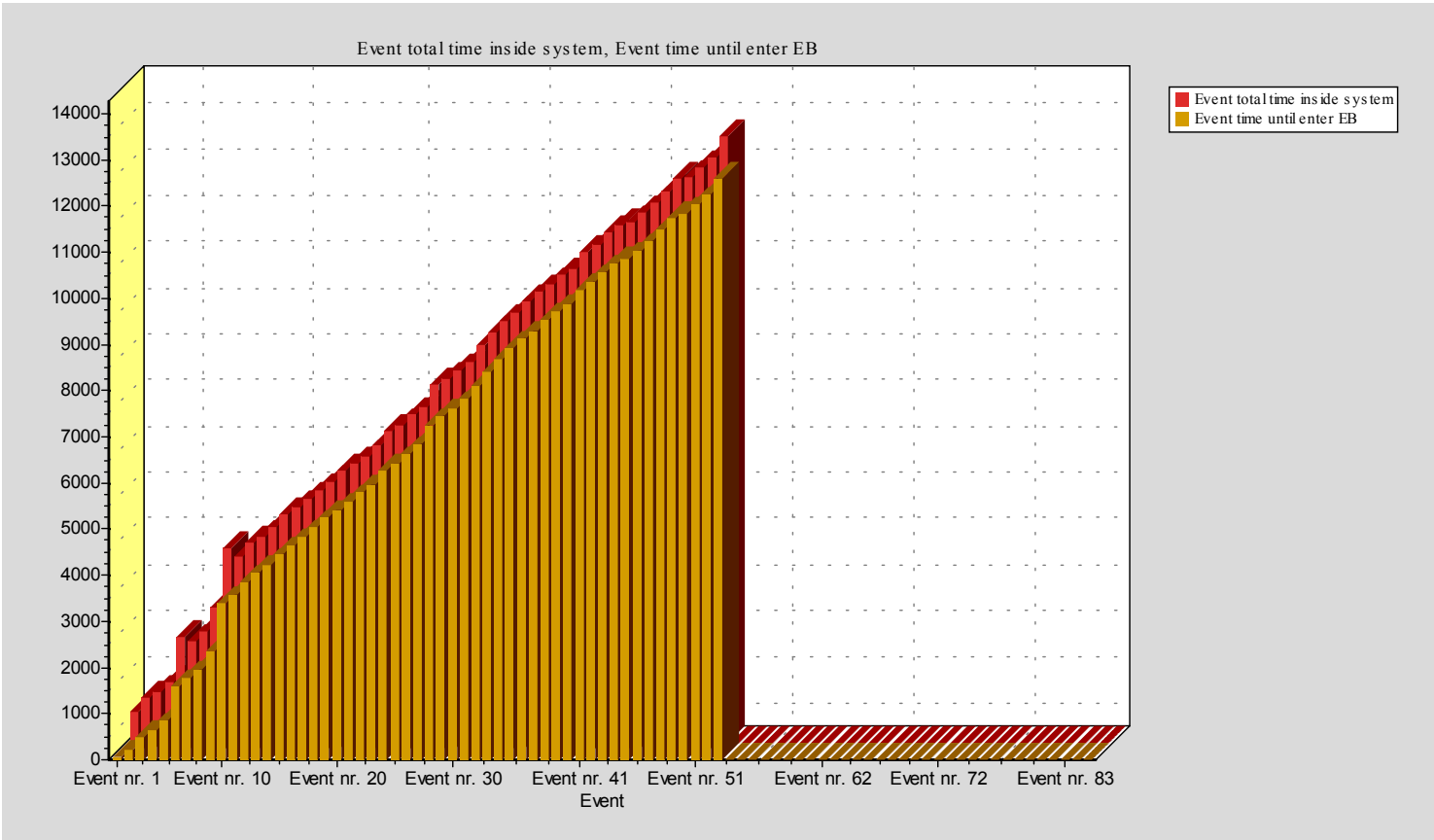



**DCC High Level Model**

# Simulation Results

## SR_ZS - DAQ 320MB/s - EB 160MB/s

### (DAQ 64b@40Mhz) - (EB 32b@40MHz)



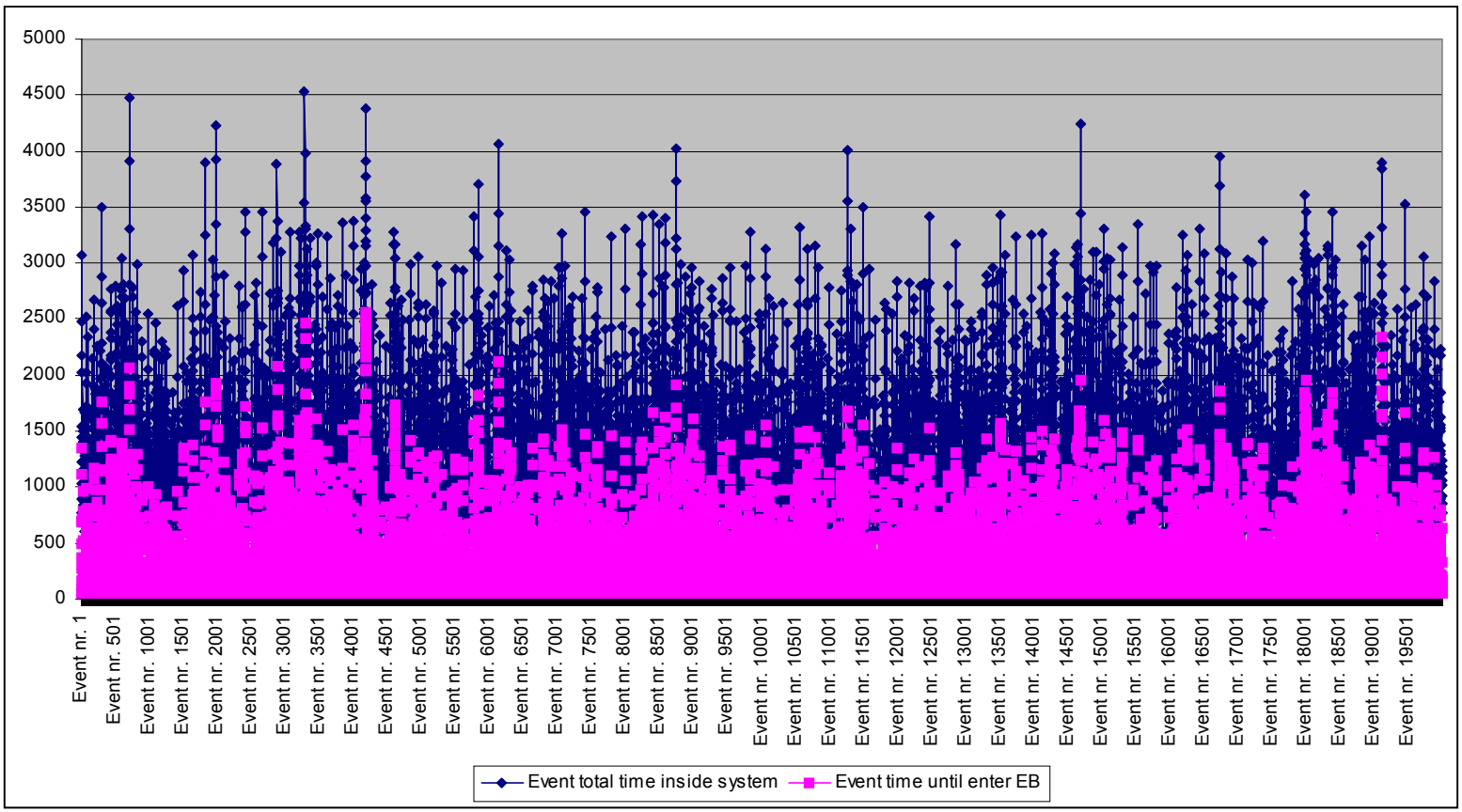



José C. Da Silva

# Simulation Results

## SR_ZS - DAQ 320MB/s - EB 320MB/s

**(DAQ 64b@40Mhz) - (EB 64b@40MHz)**



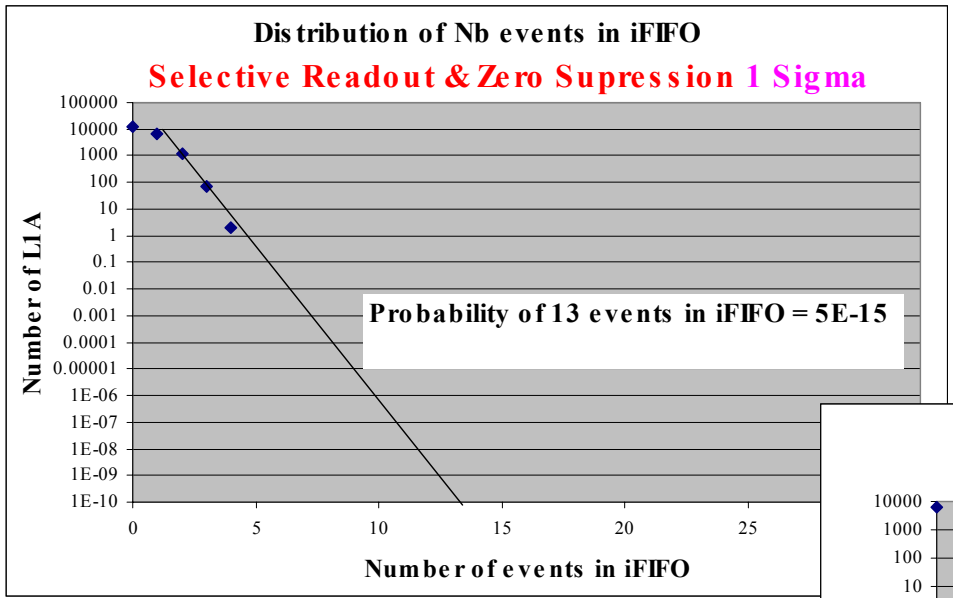

**Axis X – L1A arrival (in event numbering)**
**Axis Y – Time that each event spends in the system and time to enter EB**

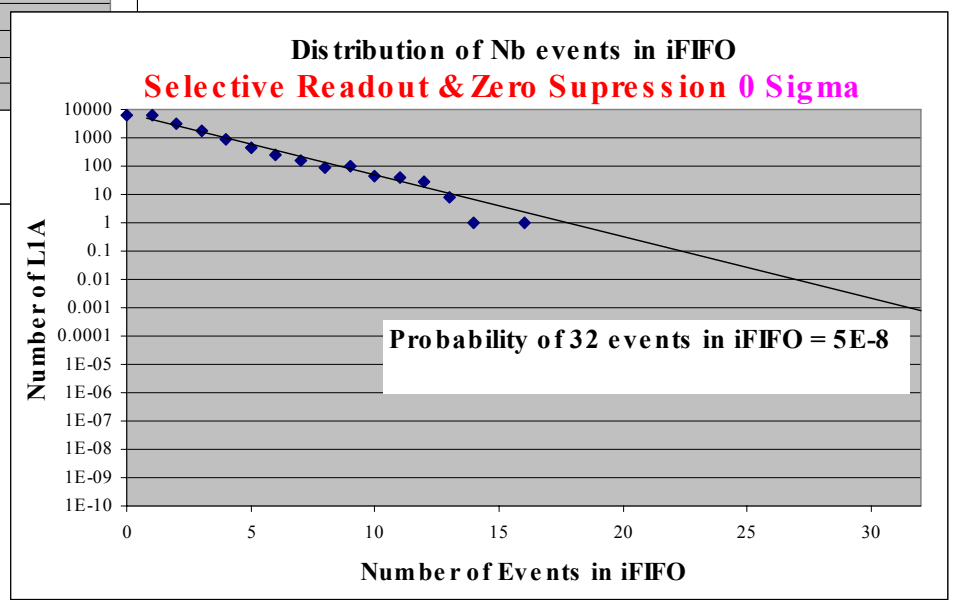
# Summary of Simulations

## PRELIMINARY RESULTS

| Data Selection | Total Event Size (average kbytes) | DCC Data Flow (average) | Simulated DCC Bandwidth (Mbyte/s) | DAQ link bandwidth (Mbyte/s) | Event Time in DCC (average microsec) | iFIFO occupancy (average nb events ) | Time to overflow | oFIFO occupancy (average kbytes ) |
|---|---|---|---|---|---|---|---|---|
| Selective Readout & Zero Spression (1σ) | 53 kByte | 95 Mbyte/s | 160 | 160 | Overflow | Overflow | | Overflow |
| | | | 320 | 320 | 14 | 0.5 | 6 years | 1.5 |
| Selective Readout & Zero Spression (0σ) | 65 kByte | 116 Mbyte/s | 160 | 160 | Overflow | Overflow | | Overflow |
| | | | 320 | 320 | 24 | 1.5 | 3 min | 2.5 |

# Overflow Probabilities



# Conclusions

1. **Detailed ORCA simulations showed that a combination of selective readout and zero suppression reduces the CMS-ECAL average data volume to the target value (100 kBytes/event).**

2. **A conceptual design of the ECAL Data Concentration Card was developed, aiming at a data throughput of 528 Mbytes/s.**

3. **Simulations of the DCC hardware, using simulated physics data as input, were used to validate the design.**

# Selective Readout Concept