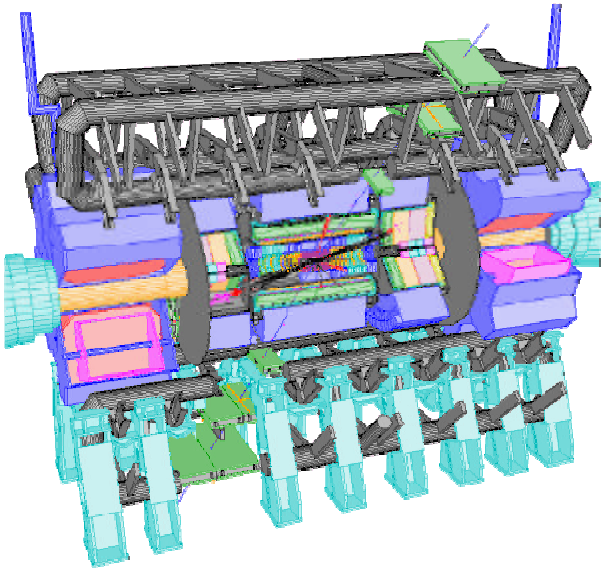


ATLAS

Status of LArG DMILL chips

C. de LA TAILLE

LAL Orsay

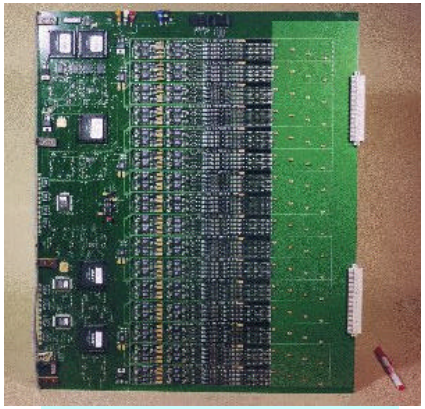
on behalf of the LArG collaboration

http::/www.lal.in2p3.fr/recherche/atlas

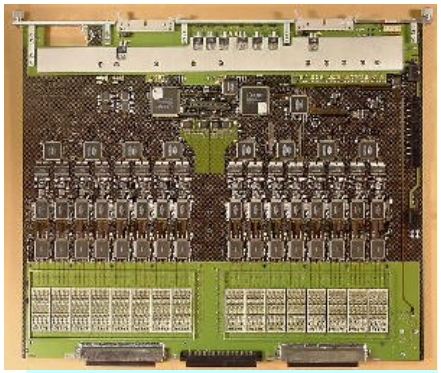
LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

Liquid Argon front-end electronics overview

[LEB6 p.265]

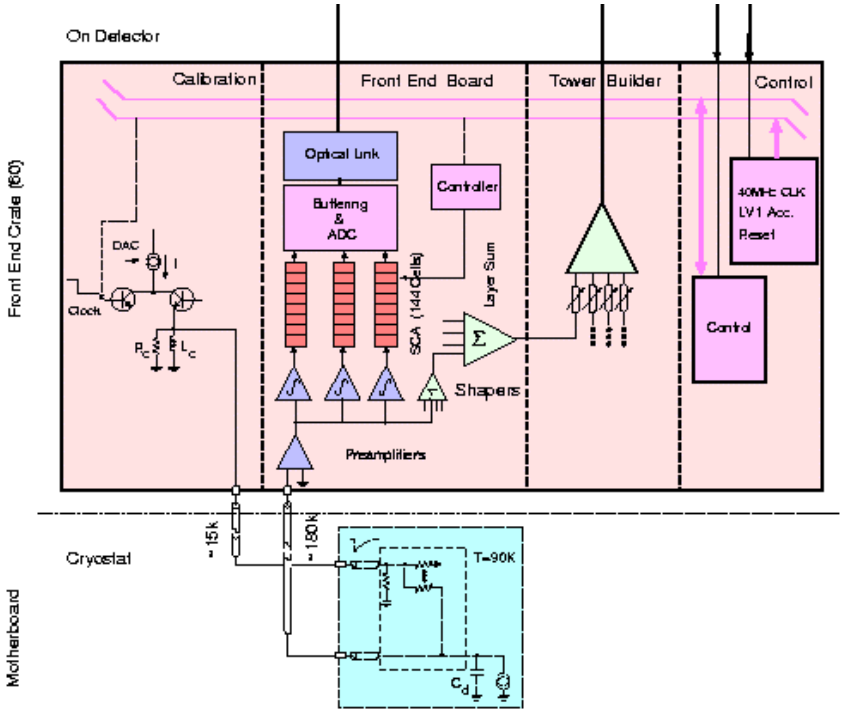


Calibration :
116 boards @ 128 ch

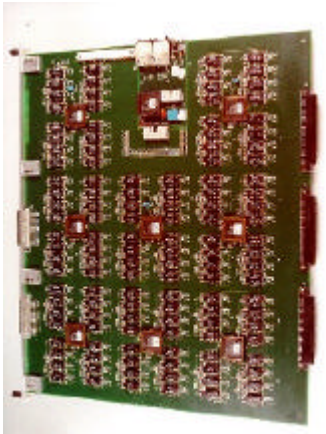


Front End Board (FEB) :
1524 boards @ 128 ch

- **On-detector electronics**
  - Boards tested functionally on mod 0
  - ATLAS *rad-tol* boards being finalized



Controller :
116 boards



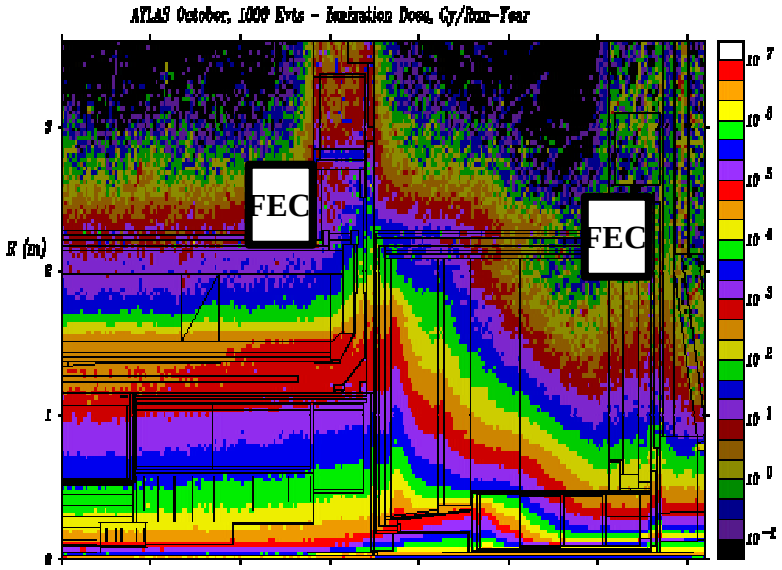
Tower builder (TBB) :
120 boards @ 32 ch

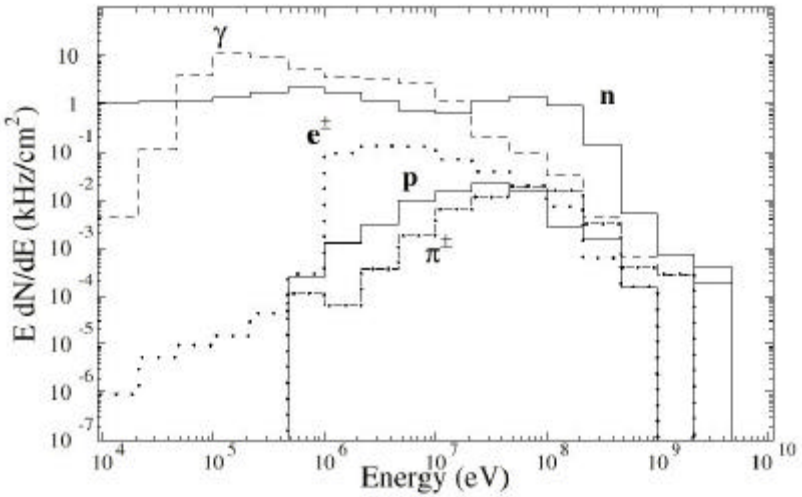
Radiation maps

[LEB6 p.270]

- **Radiation levels for LAr crates**
  - barrel (in 10 yrs) :
    - TID = 50 Gy/10yr
    - NIEL = 1.6 10^{12} N/cm^2/10yr
    - SEE = 7.7 10^{11} h/cm^2/10yr (>20 MeV)

- **Radiation Tolerance Criteria (RTC) for DMILL chips (includes SF)**
  - TID = 50 * 3.5 (simul) * 1.5 (ldr) * 2 (lot)
    = 525 Gy/10yr (3.5 kGy for COTS)
  - NIEL = 1.6 10^{12} * 5 (simul) * 1 (ldr) * 2 (lot)
    = 1.6 10^{13} **N/cm^2/10yr** (3.2 10^{13} for COTS)
  - SEE = 7.7 10^{11} * 5 (simul) * 1 (ldr) * 2 (lot)
    = 7.7 10^{12} **h/cm^2/10yr**
  - Irradiation tests are *mandatory* for final qualification and still *recommended* for production batches

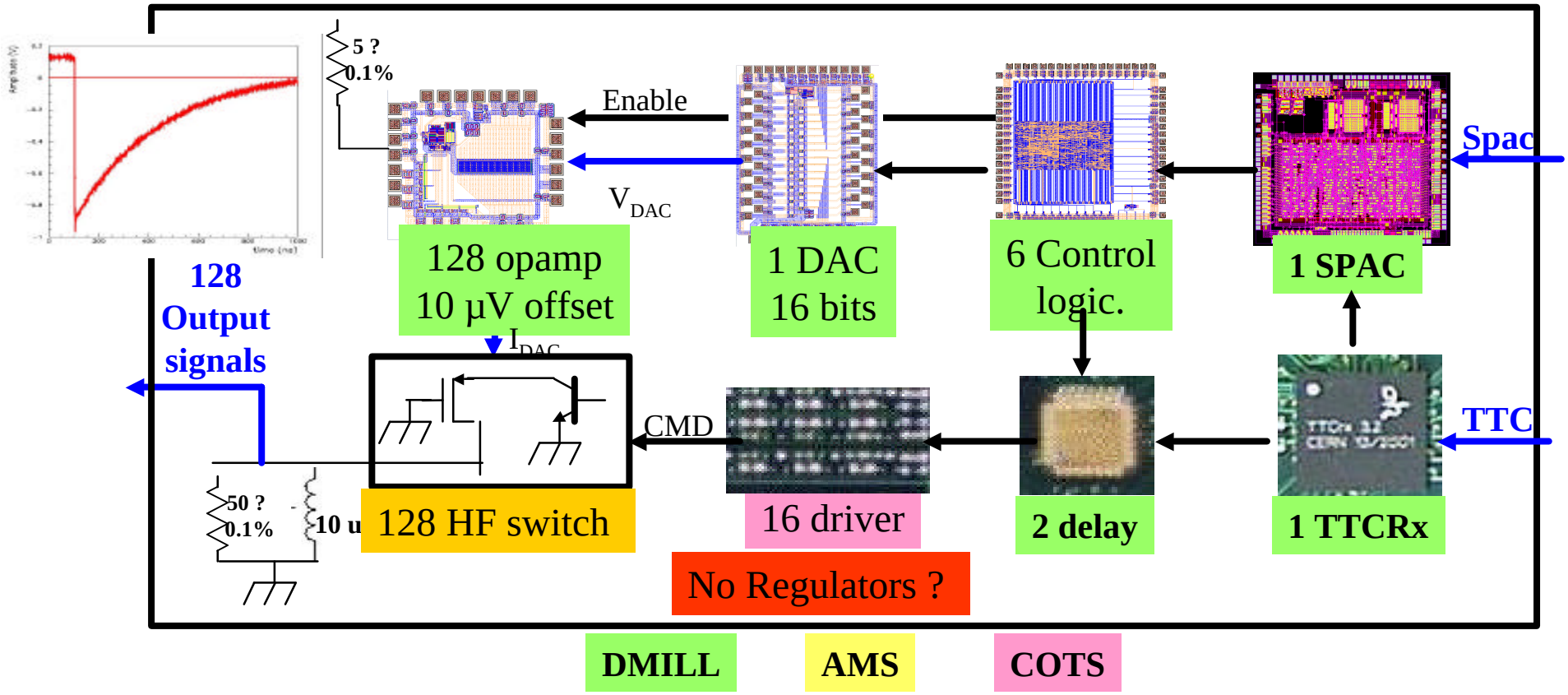




Calibration Board : overview

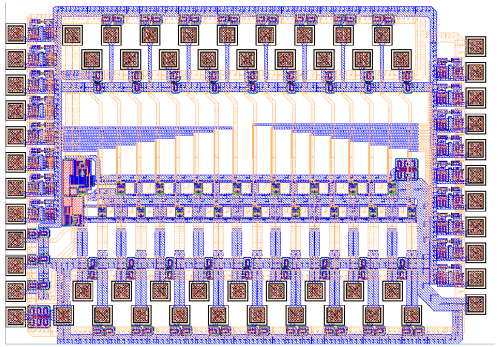
[LArG 2000-006]

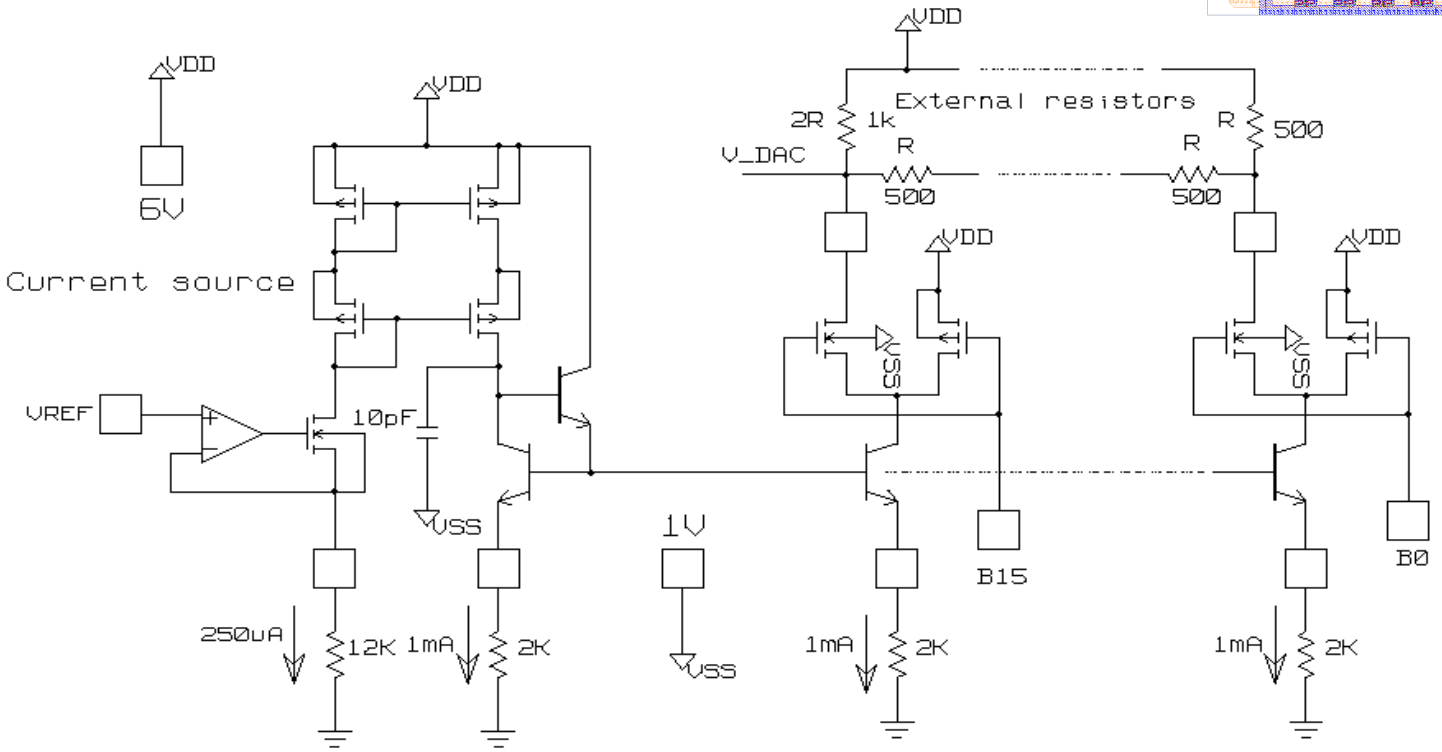
- **Generate 0.2% precision calibration pulses** (Annecy, Mainz, Orsay)
  - Milestones : * Final prototype : Apr 02
    * Production of 130 boards : Apr 03
    * Installation complete Feb 05



Calib : DAC design

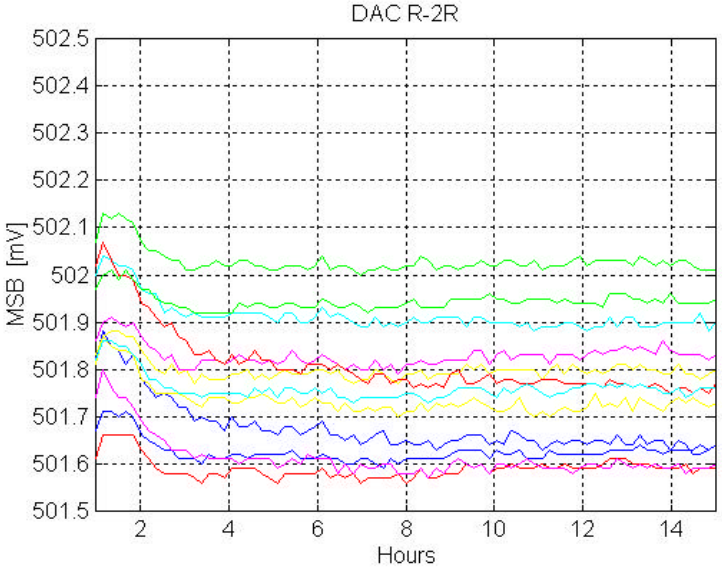
- **16 bit DAC : DMILL (Orsay)**
  - COTS failed irradiation tests at 20 Gy
  - 16 bits dynamic range (16 µV-1V), 10 bits accuracy (0.1%)
  - external R/2R ladder and highly degenerated current sources
  - Good stability at small DAC value

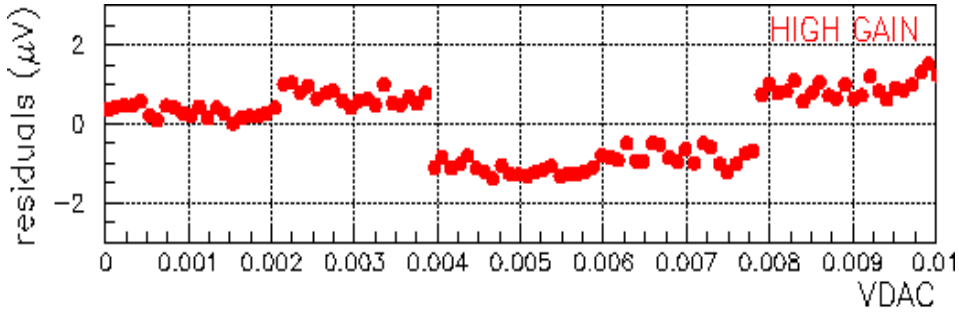


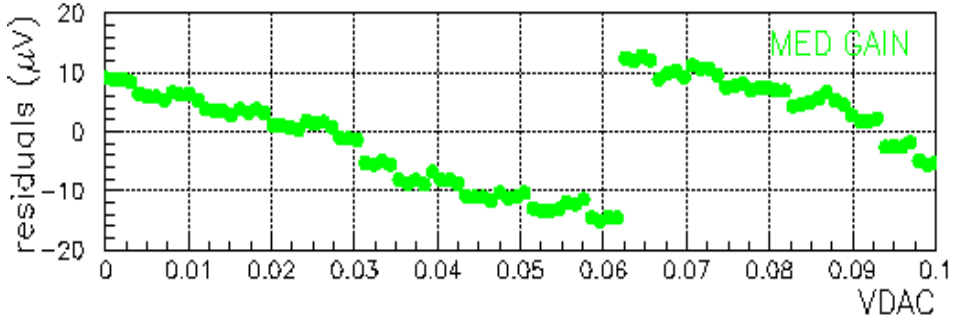


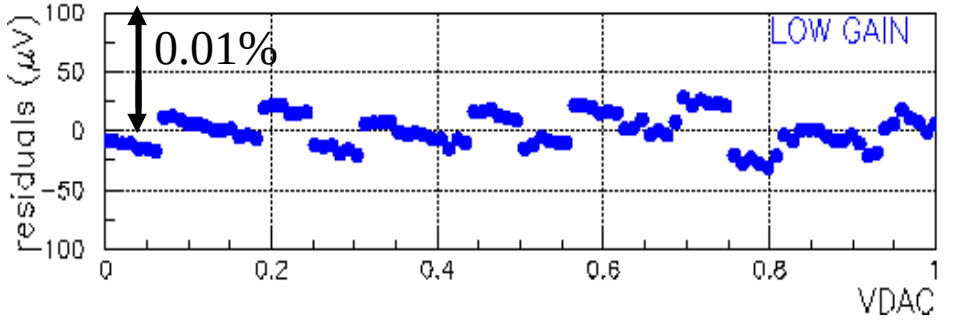
Calib : DAC performance

- **Yield :**
  - 6.3 mm^2 chip, received Mar 01
  - yield : 94%
- **Performance :**
  - Accuracy : 0.01% or 10 µV
  - Linearity : INL < 0.01%
  - Stability : 0.01%/K
  - Settling time < 1 µs



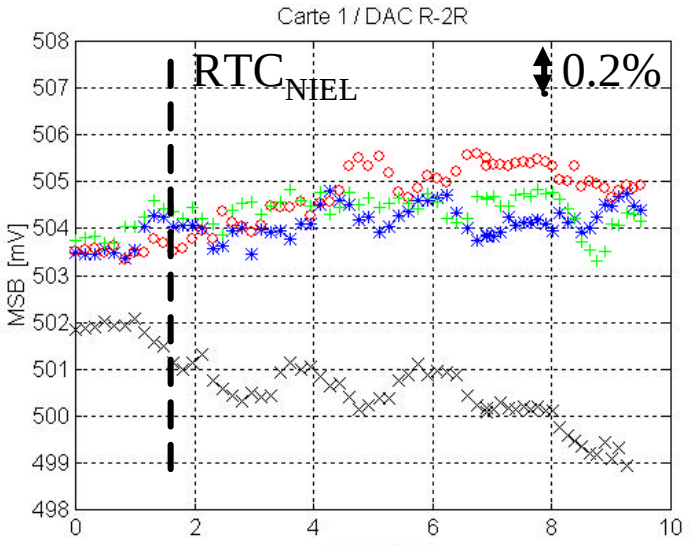


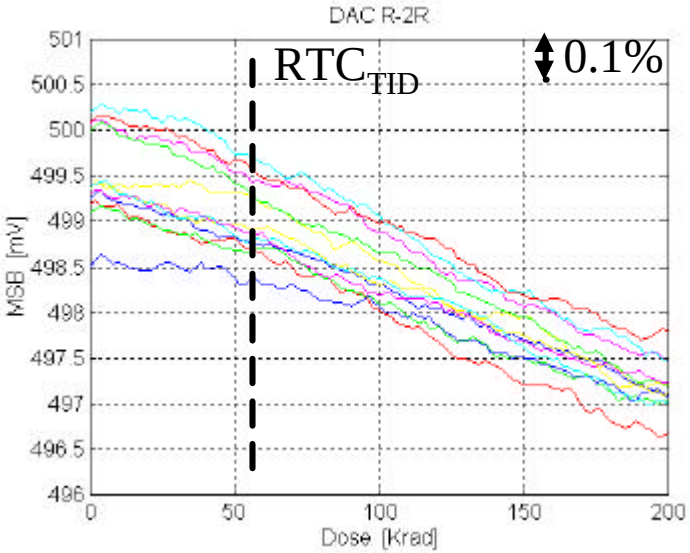


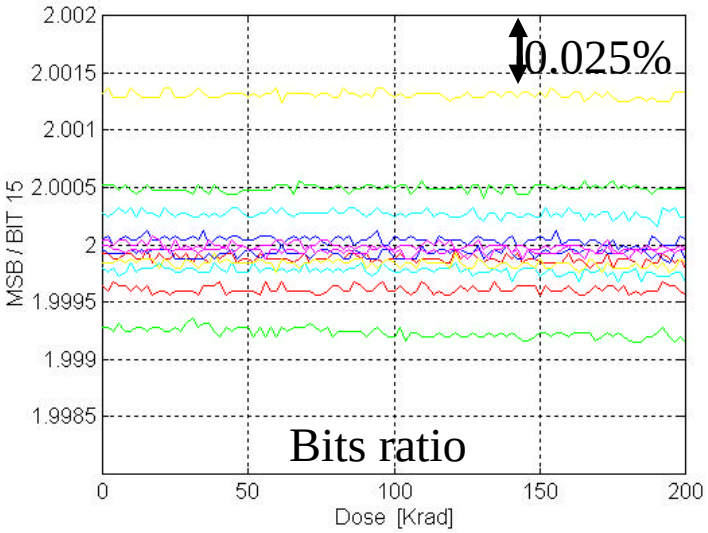


Calib : DAC irradiation results

- **Neutrons : up to 9 10^{13} at CERI**
  - No significant change
- **Gammas up to 2 kGy with ^{60}Co**
  - 0.5% overall change after 2 kGy
  - Global shift in current reference due to current mirror
  - V_T shift mismatch around 1 mV
  - Good annealing

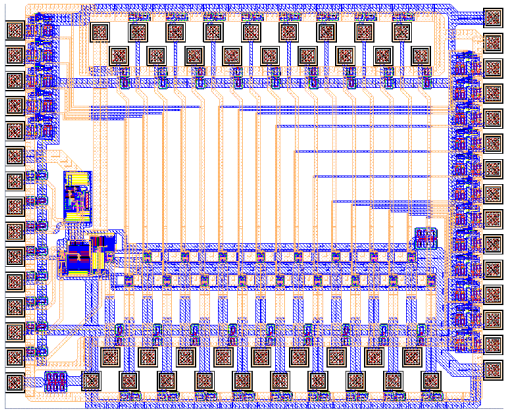


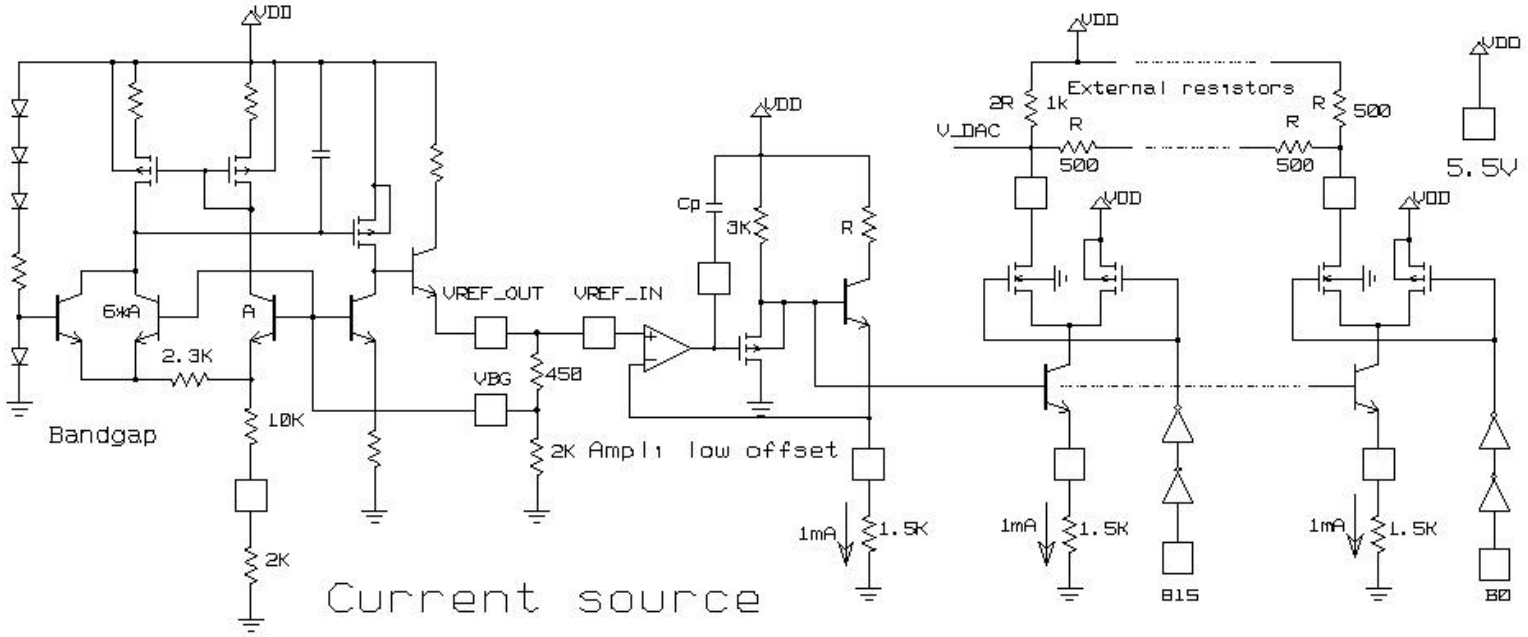




Calib : DAC final version

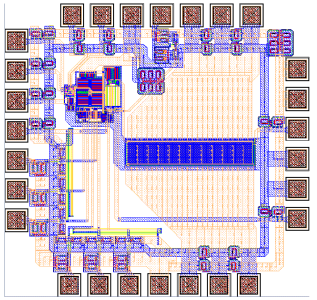
- **Final DAC prototype**
  - Band-gap reference voltage (1.5 V).
  - Current mirror removed. Feedback on reference.
  - Logic level translators inside
  - Submitted in Sept 01, area : 8 mm^2
  - 1 DAC per board, 150 chips needed

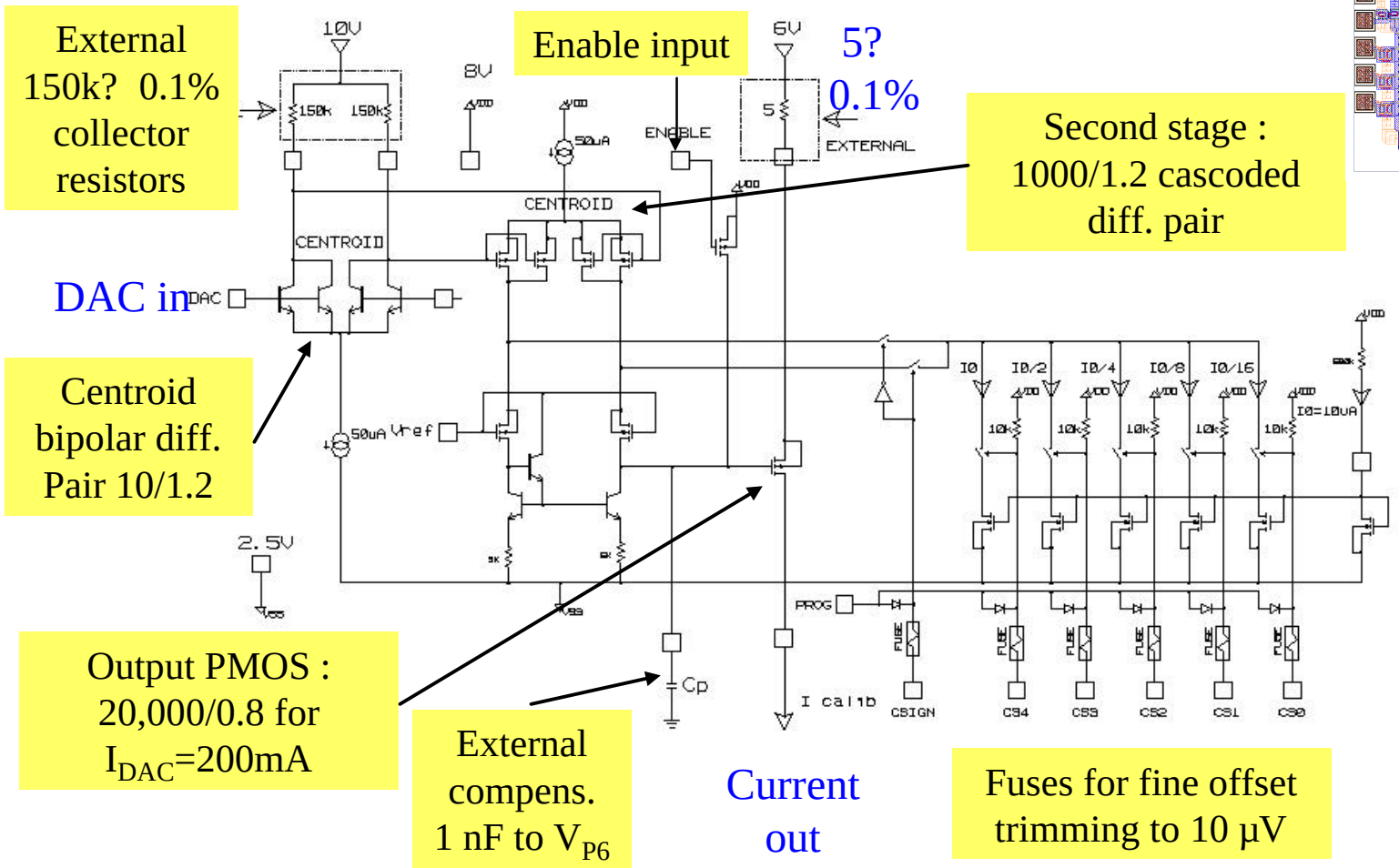




Calib : low offset opamp design

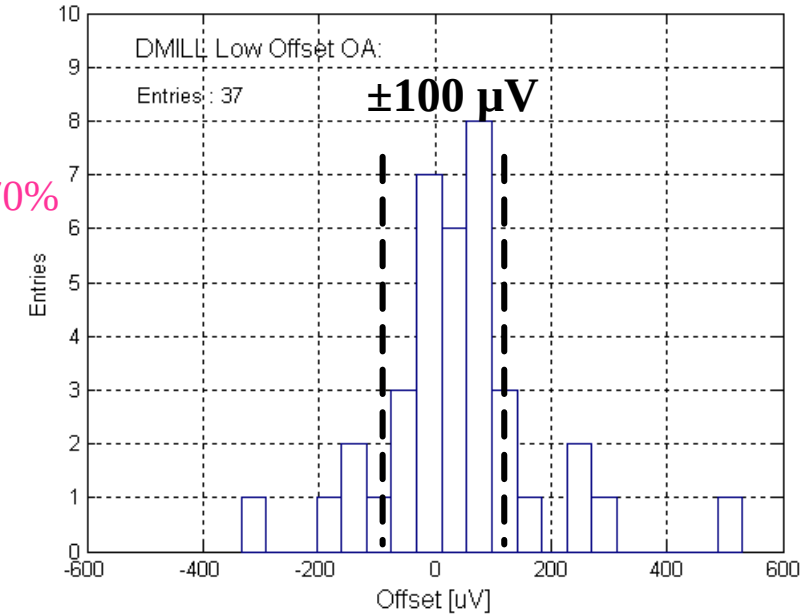
- **Used in 0.2% accuracy DC current source** (2 µA-200 mA) **(Orsay)**





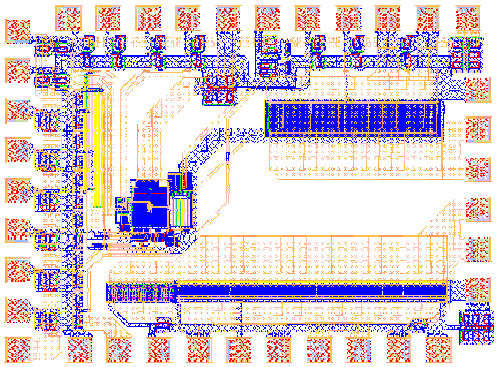
Calib : low offset opamp performance

- **Yield :**
  - 2 mm^2 chip, received March 01 (MPW 471).
  - Fully functional. Yield : 92%
  - Selection inside ±100 µV ? sorting yield : 70%



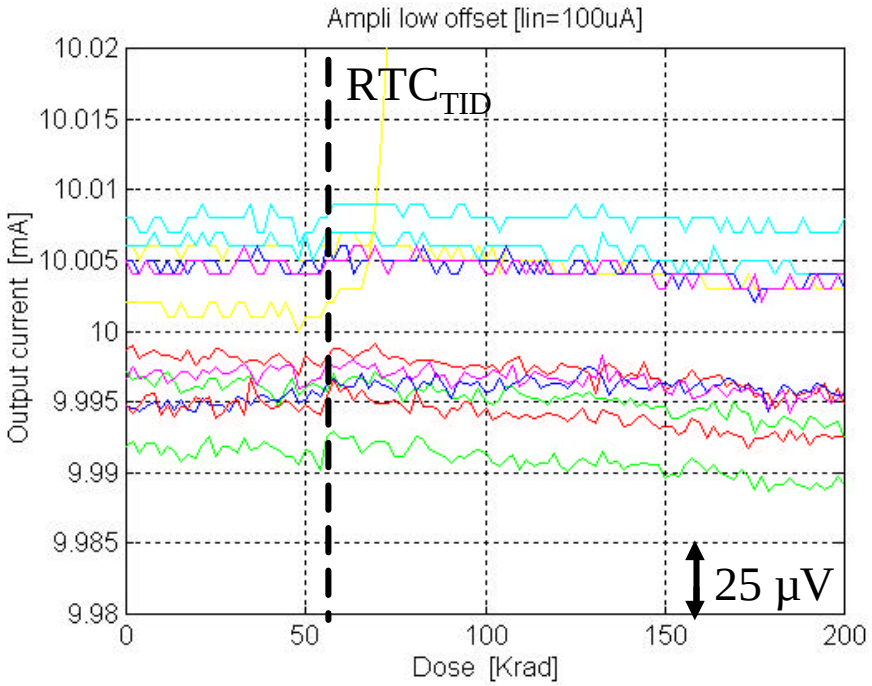
- **Performance :**
  - Open loop gain 80,000
  - GBW = 100 kHz
  - Offset stability : a few µV
  - Temperature sensitivity : +1 µV/K

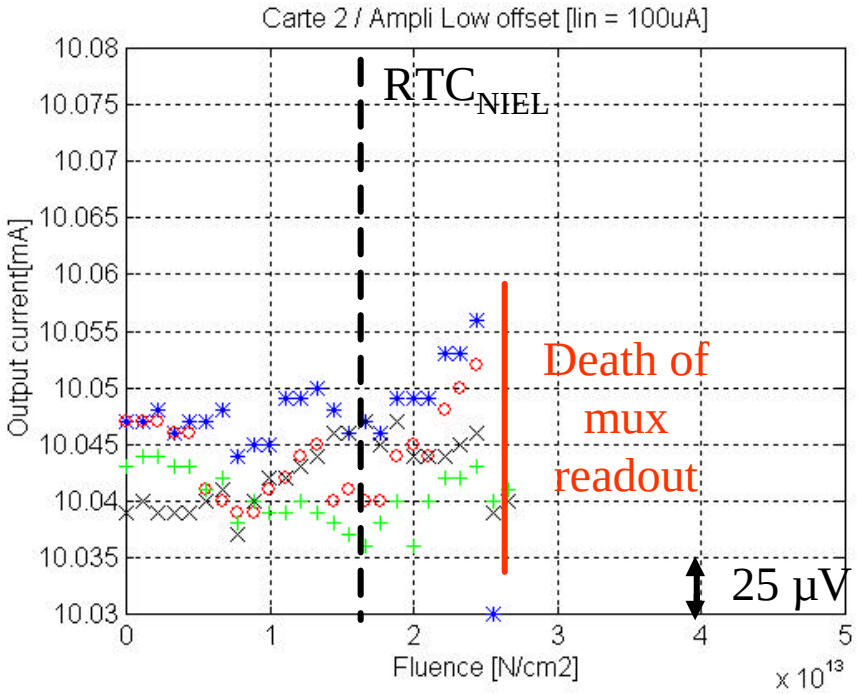
- **Final iteration**
  - Include HF switch (cost reduction)
  - Opamp unchanged
  - Chip submitted in May 01. Area : 3 mm^2



Calib : low offset opamp irradiation results

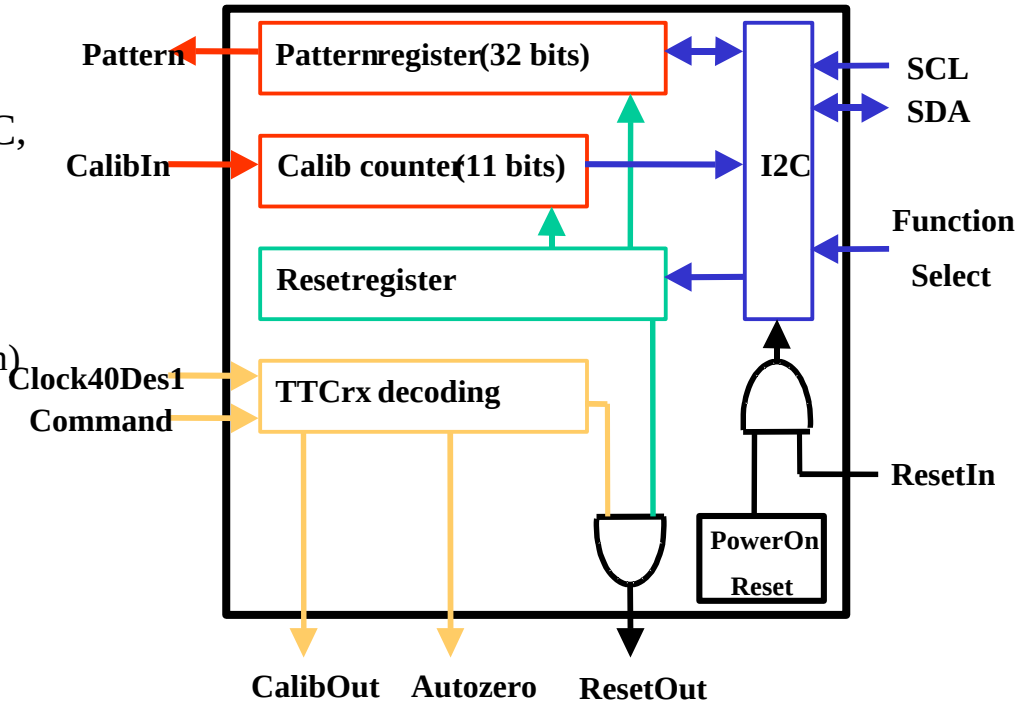
- **Gammas up to 2 kGy**
  - ^{60}Co at Pagure (Saclay)
  - No change within 15 µV up to 200 krad
- **Neutrons up to 9 10^{13} N/cm^2**
  - ~10 MeV neutrons at CERI (Orleans)
  - Maximun change : 50 µV after 9 10^{13}
  - Beta change (@I_C = 25 µA) :
    - 180 prerad, 62 @ 5$10^{13}$, 37 @ 9 10^{13}

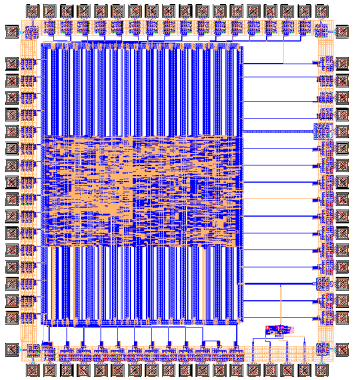




Calib : Digital chips

- **Control logic : DMILL** (Annecy)
  - Common DMILL chip to control DAC, pattern and delays registers
  - 16 mm^2 chip, received Mar 01 (MPW 471). Yield : 80%
  - SEE test performed in Apr 01 (Louvain)
    - no SEU up to ~3. 10^{12} p^+ (60 MeV)
    - In ATLAS < 2 SEU/yr
  - Iterated in May 01 to correct initialization

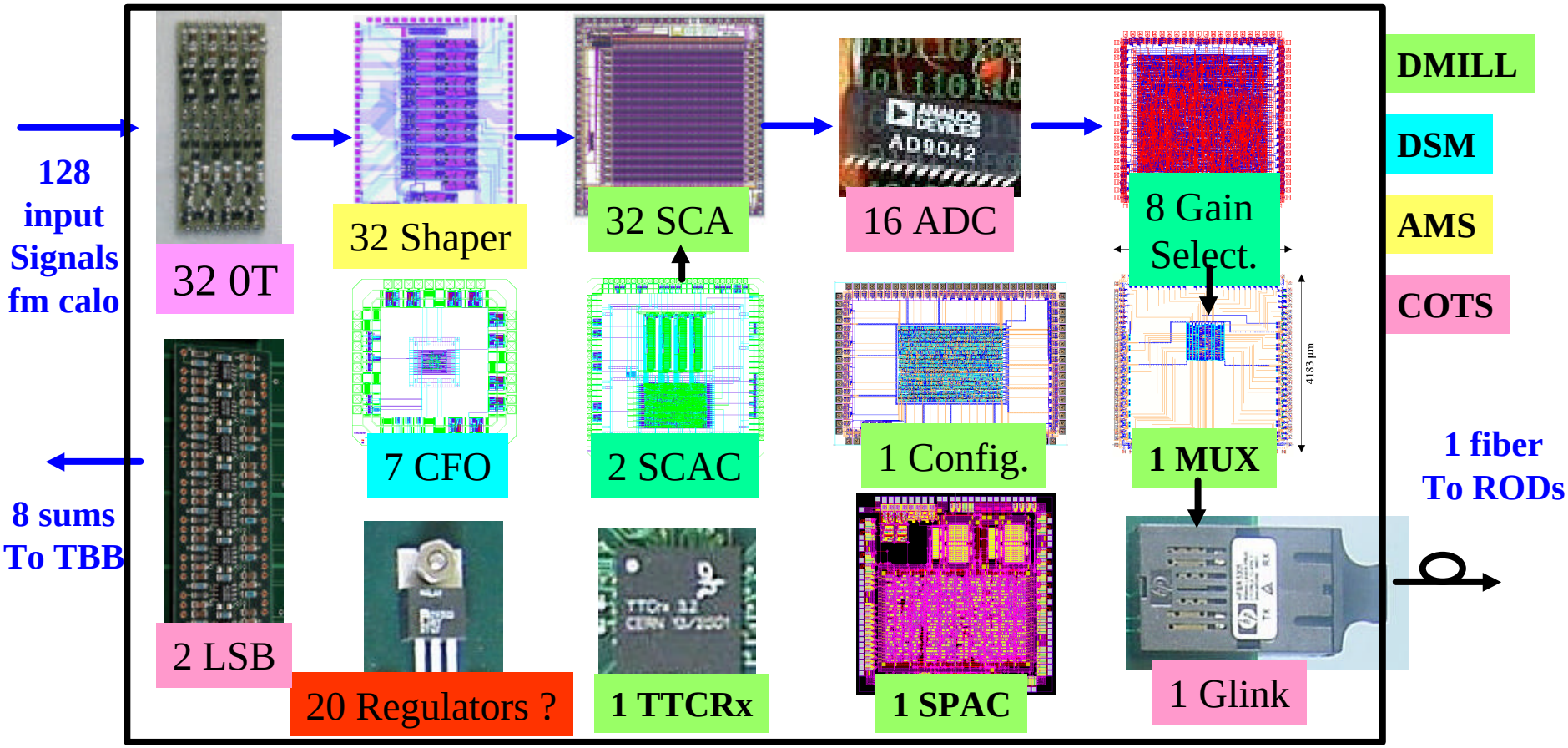




- **Delay chip : DMILL** (CERN)
  - 2 chips per board ? 260 chips required

Front End Board (FEB) : overview

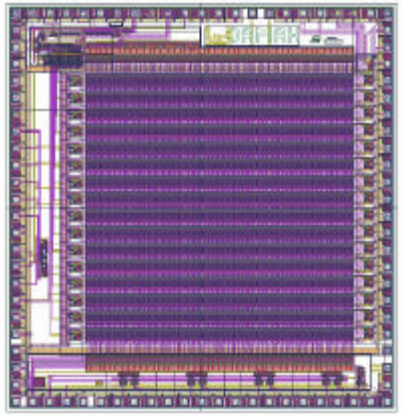
- **Amplification, shaping, analog storage and digitization** (Nevis)
  - Milestones : first final board : Oct 2001, 30 boards : Oct 2002, 1700 boards : Apr 2003



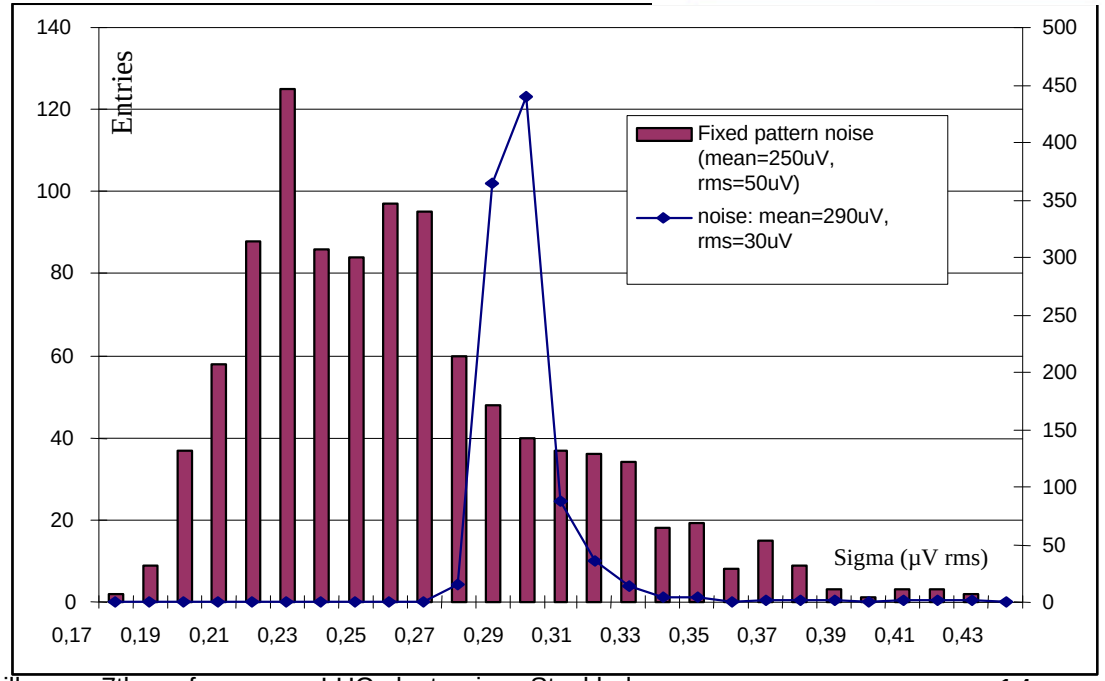
FEB : analog pipelines (SCA)

[LEB6 p.203]

- **SCA : DMILL CMOS chip** (Nevis,Orsay,Saclay)
  - 144 cells deep analog storage, 13 bit dynamic range
  - 4 channels (3 gains + 1 reference) per chip. Dissipation 300 mW.
  - Simultaneous Read/Write at 40 MHz. Output rate 5 MHz.
  - Noise : 290 µV ; fixed pattern noise : 250 µV ; jitter < 70 ps
  - Irradiation tests : OK
    - 3 kGy
    - 2 10^{13}N
    - no SEU tests
  - Yield : 10-90%

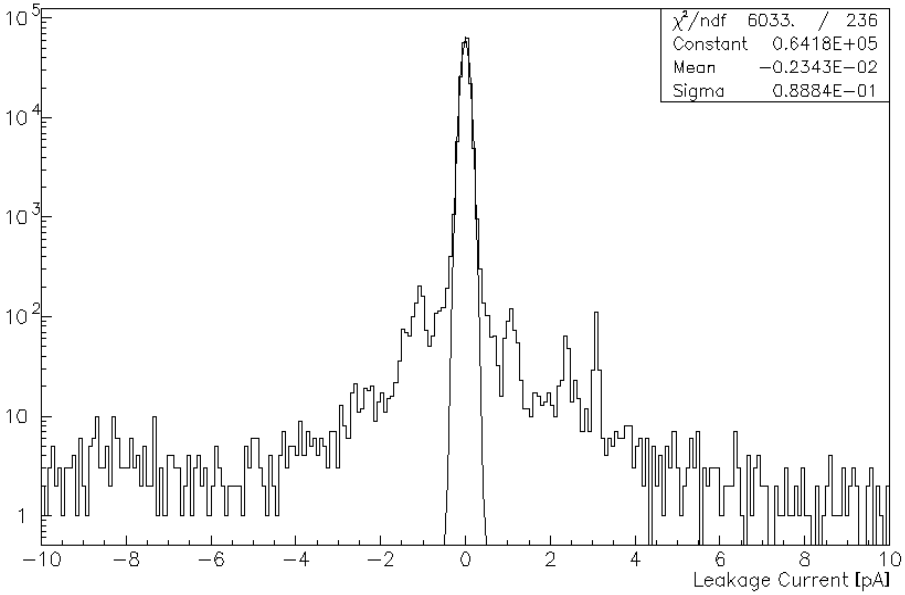


BATCH	DATE	YIELD
V 1.1	6 / 98	90 %
V 1.2	8 / 98	80 %
V 2 w12	8 / 99	50 %
V2 w4	8 / 99	84 %
V 3.1	10 / 99	10 %
V 3.2	7 / 00	65 %
V 4.1	3 / 01	60 %



FEB : DMILL SCA test results

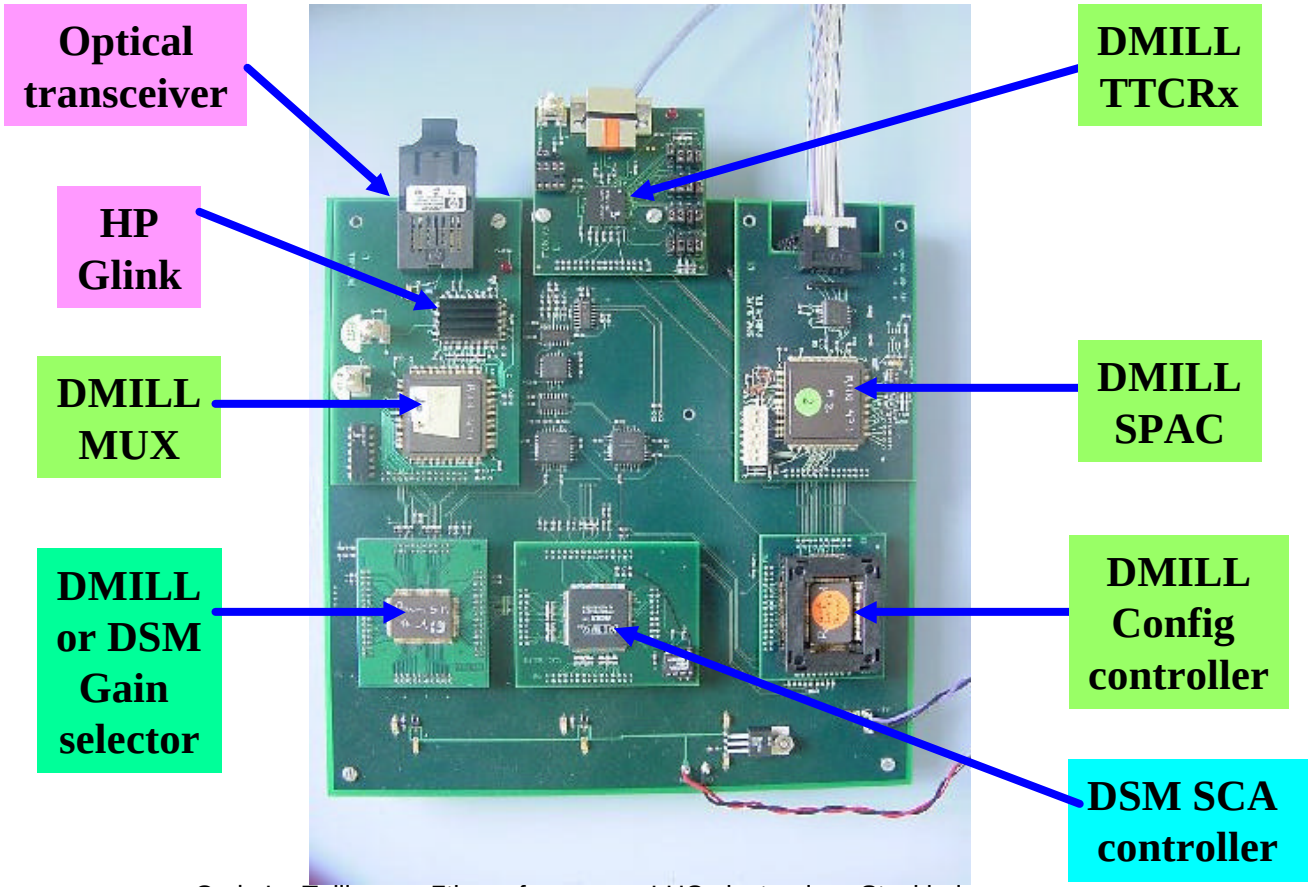
- **Engineering run launched in nov 00**
  - 30 mm^2 chip; 416 chips/wafer
  - 6 wafers received in march 2001, 2 more in july 01 (new batch)
  - 2543 chips tested : raw yield : 69%
  - Cut on leakage current : I < 5 pA ? **yield : 65%**



- **Production run : fall 2001**
  - 32 per FEB ? 54,000 chips needed
  - 220-250 wafers (~ 1.5 M$)
  - PRR with Atmel : Oct 2001. Define target yield
  - Tests at Grenoble with robot : ~6 months

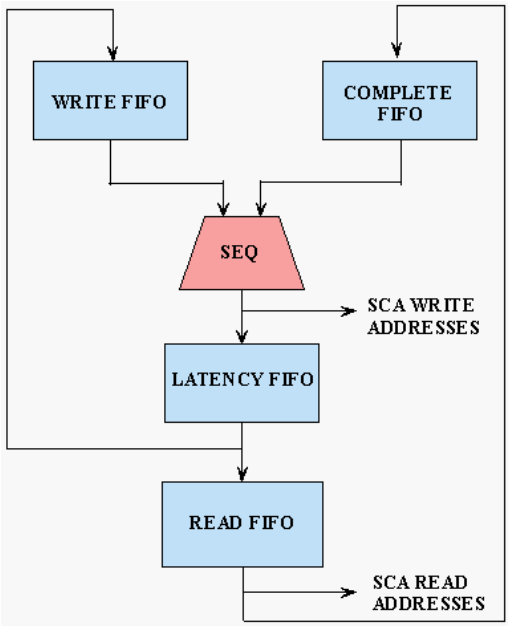
¼ digital FEB

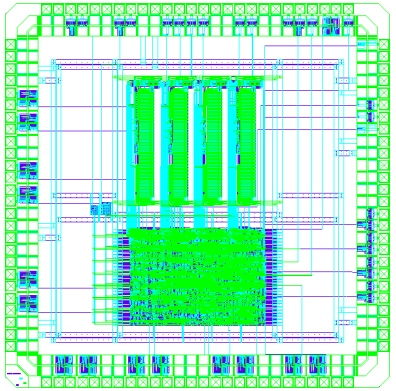
- **Test setup for all FEB digital ASICs** (Nevis)
  - Complete operation of SCAC, Gain selector, config contr., SPAC slave, TTCRx, MUX, Glink ? **Tests OK**



FEB : SCA controller (SCAC)

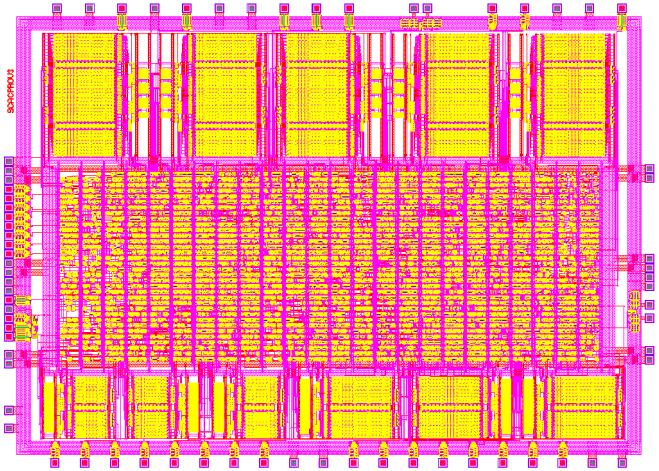
- **A very critical component** (Alberta)
  - Book-keeping of SCA addresses
  - Mod0 Xilinx (0.35 µm XC 4036) failed at 450 Gy
    - SEU cross-section : $s_{SEU} = 2.7\ 10^{-9}$ cm^2 [LArG 2001-011]
    - LET for configuration switches : 22 ±2 MeV
    - 1 latch-up @105MeV : $s_{SEL} = 8\ 10^{-14} - 10^{-12}$ cm^2 (95% CL)
- **Difficult implementation in DMILL**
  - Special RAMs needed (CEA-DAM)
  - Large chip area (80 mm^2) ? potentially low yield (20%)
  - SEU : incorrect functioning until reset
    - no room for error detection/correction
  - Submitted Nov 00 (MPW 533), received July 01
- **Backup launched in DSM (0.25 µm)** (Nevis)
  - Smaller area (16 mm^2), higher yield, lower cost
  - Error correction implemented
  - Submitted Feb 01, received July 01.
- **In critical path if an iteration is needed**
  - 2 chips per FEB, 3 400 chips needed





FEB : DMILL SCAC test results

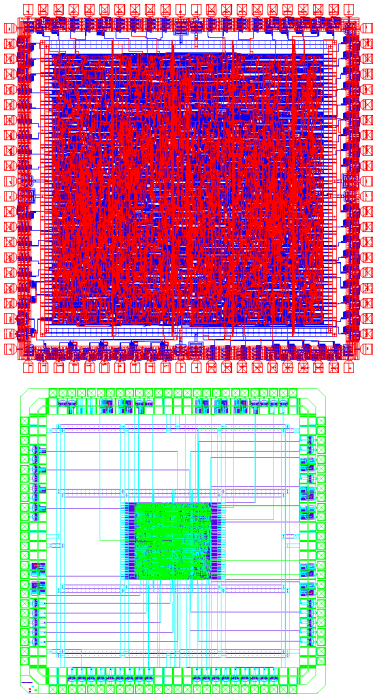
- **Yield** (DMILL)
  - 40 chips received july 01
  - 28 good parts : preliminary yield : 70%
  - Correct operation up to 50 MHz (9 chips tested)
  - No failure after burn-in (7 chips tested)



- **SEU test results** (Alberta)
  - 4 chips irradiated to 3-6 10^{11} p^+/cm^2 (74 MeV) (Triumf Aug 01)
  - Associated TID : 30-80 krad
  - Mean flux until upset : 4.6 ± 0.2 10^{10} p^+/cm^2. Power cycling needed to reset !
  - Extrapolated to ATLAS as 1 SEU/SCAC/70days ? reset every hour
  - Traced to “Power on reset” (analog) circuit, issuing continuous reset.
    - Failure probably due to TID effect
    - Removed externally
    - Further failures (with TID) of the input LVDS buffers

FEB : Gain selector

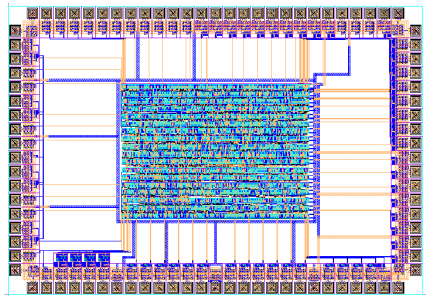
- **Gain selection and data formatting** (Nevis)
  - On chip storage of 16 thresholds values
  - SEU mitigation : on chip bit error detection and correction
  - **DMILL chip**
    - 21 mm^2 chip, received Mar 01. yield : 93%.
    - 581 chips per wafer, 34 wafers necessary : full engineering run.
  - **DSM alternative**
    - 16 mm^2 chip, submitted in Feb 01, received Jun 01
- **SEE irradiation results (DMILL chip)**
  - 5 chips irradiated to 2-7 10^{13} p^+ (50, 100, 158 MeV) (Harvard may 01)
  - SEE : SBE (corrected) and SEU (? 1-2 events corrupted)
  - Extrapolated rate to full calo : 1 SBE/30 min 1 SEU/168 min



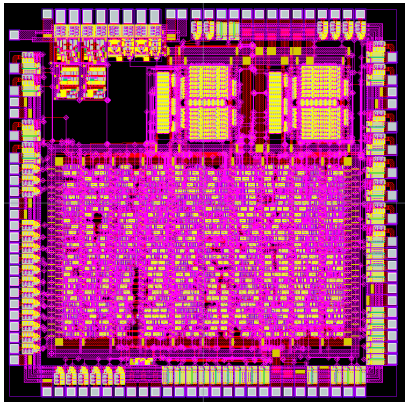
Energy	Fluence	Single Bit Errors (SBE)		Single Event Upsets (SEU)	
(MeV)	(10^{13}/cm^2)	Number	σ (10^{-13}cm^2)	Number	σ (10^{-13}cm^2)
50	2.4	0	-	0	-
100	4.0	14	3.5	4	1.0
158	20.8	212	10.2	38	1.8

FEB : digital chips

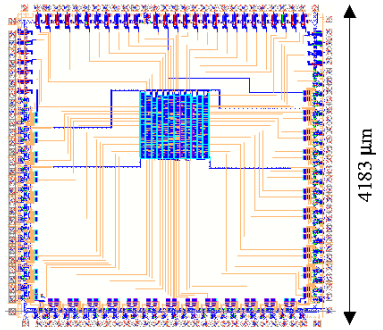
- **Config controller** **(Nevis)**
  - Interfaces SPAC to local busses (shaper, SCAC, regulators…)
  - DMILL chip : 22 mm^2 area, received Mar 01 yield : 93%. Final
  - SEE irradiation results (4 DMILL chips) 7-22 10^{13} p^+ (158 MeV)
    - 69 SEU observed ? $s_{SEU} = 1.5\ 10^{-13}\ cm^2$
    - R_{SEU} = 1 SEU/26.8 hr in ATLAS (2-15 Mrad associated TID)



- **SPAC slave** **(Paris)** [LEB6 p.454]
  - Serial interface to write/read parameters. Manchester encoding
  - 27 mm^2 DMILL chip, received Mar 01. yield : 94%.
  - Iterated in sept 01 for SEU mitigation

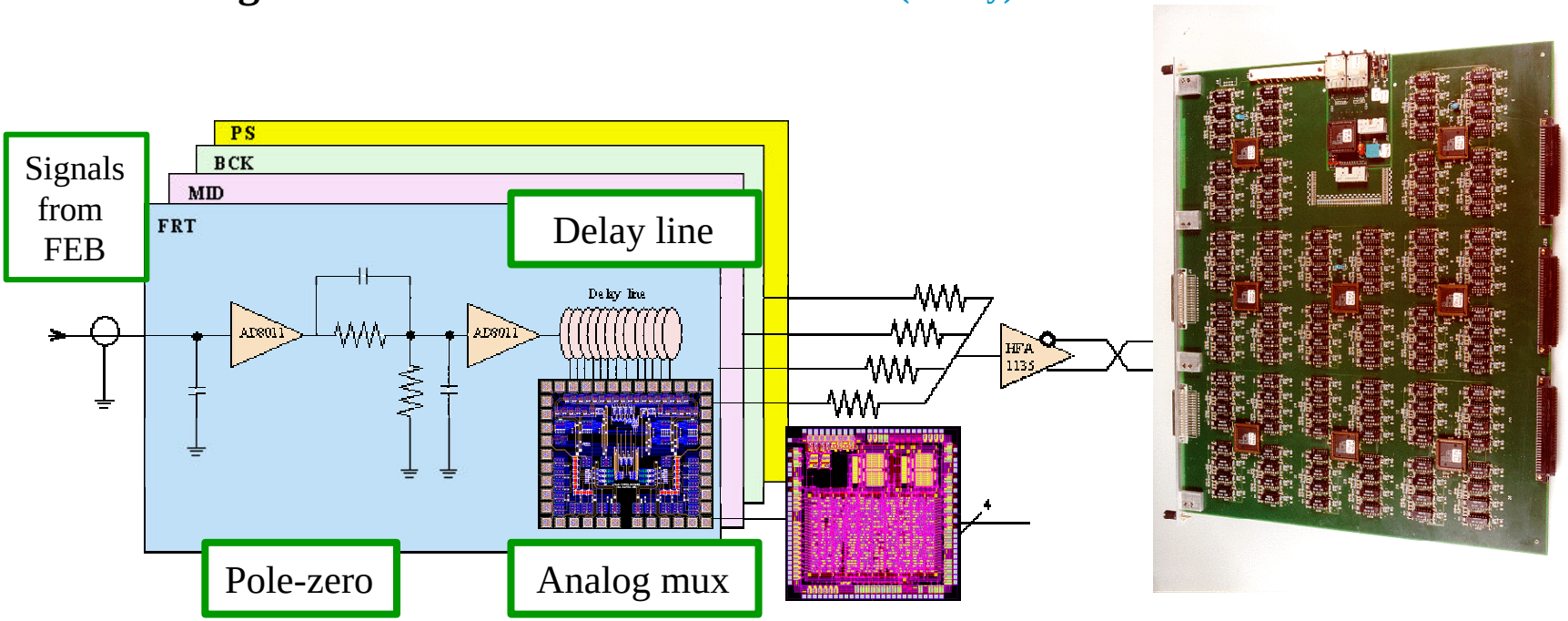


- **MUX (Multiplexer)** **(Grenoble)** [cf. talk by D. Dzahini]
  - Data formatting for Glink serializer (32bits 40MHz ? 16bits 80MHz)
  - 18 mm^2 chip, received Mar 01. yield : 88%.
  - SEE test up to ~ 10^{13} N (20 MeV) : negligible compared to Glink
  - Iterated in may 01 to remove dual mux for single Glink



Tower builder : overview

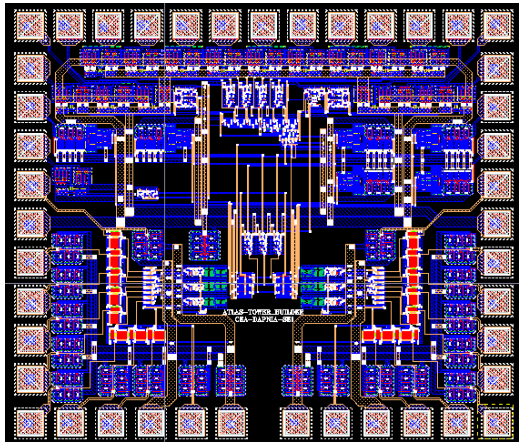
- **Analog summation to form LVL1 towers** (Saclay)



- **Milestones :** same as calib
  - Oct 02 : 2 final boards
  - Dec 02 : PRR

TBB : analog multiplexer

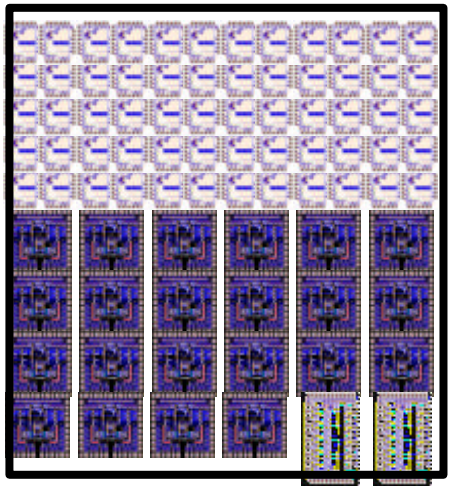
- **Analog multiplexer (BiMUX) : DMILL (Saclay)**
  - previous COTS (DG358) failed at 170 Gy
  - Prototype DMILL chip realized in 1998
    - 8 big CMOS switches + control logic (registers)
  - area : 4.6mm^2 ; yield : 80%
  - 32 chips per board ? 8,000 chips needed
  - Irradiated to 2 kGy and 310^{13} N.
  - SEU test showed no error up to ~ 10$^{1?}$ N (20 MeV)
  - Full production planned in 2001 or 2002



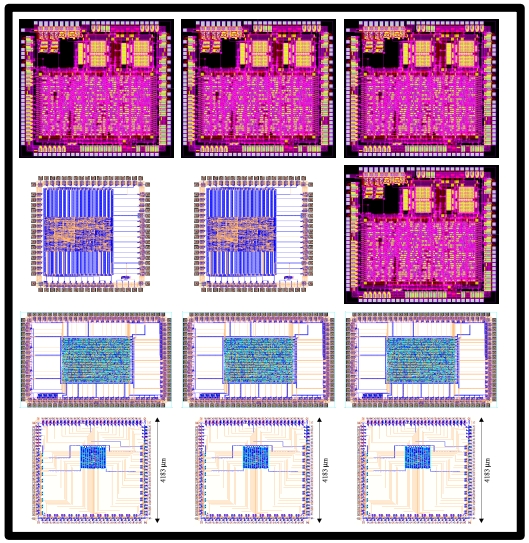
Shared DMILL wafers

- **Analog reticle**
  - 52 opamps
  - 25 BiMUx
  - 2 DAC
- **13 wafers needed**
- **Cost : ~ 150 k$**

- **Digital reticle**
  - 4 SPAC
  - 2 calib logic
  - 3 Configuration controllers
  - 3 MUX
- **20 wafers necessary**
- **Cost : ~ 200 k$**



18 mm



Summary of LArG DMILL chips

Chip	Area (mm^2)	Min chips required	OK /tested	Yield	Iteration out	Comments
SCA	30	54 000	1643/2543	65%	None	final
Gain select.	21	13 300	27/29	93%		DSM alternative
SCA contr.	80	3 300	28/40	70%		DSM alternative
FEB config	20	1 650	37/40	93%	None	final
DMUX	18	1 650	15/17	88%	nov 01	Remove dual
Calib logic	16.4	700	3/3	100%	nov 01	Fix initialization
SPAC slave	27	2 500	17/18	94%	feb 02	Mitigate SEU
Opamp	3	17 000	26/37*	70%*	nov 01	Add HF switch
DAC	6.3	130	18/19	94%	feb 02	Fix reference
Delay	6.5	260			None	final
TTCRx		2 100			None	final
BiMUX	4.6	8 320	65/80	81%	None	final

* within ± 100 µV

Summary

- **10 DMILL chips designed and produced in 2000-2001**
  - 3 MPW (MPW 471, MPW 511, MPW 533)
  - 1 full engineering run (SCA)
- **7 digital chips**
  - **Yield > 80%**
  - All designs final
  - 2 chips have 0.25 µm DSM alternatives (SCAC, Gain select.) ? **Choice in Oct 01**
- **3 analog chips**
  - Good performance (offset, leakage…)
  - **Yield > 65%**
- **250 wafers needed for ATLAS in 2002**
  - ~ 200 for the SCA, PRR in oct 2001
  - 33 shared wafers for 8 different chips : packaging issues