TTCPR: A PMC Receiver for TTC

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Abstract

The TTCPR receiver is a mezzanine card intended for use in distributing TTC information to Data Acquisition and Trigger Crates in the ATLAS Prototype Integration activities. An original prototype run of these ~cards was built for testbeam and integration studies, implemented in both the PMC and PCI form factors, using the TTCrx chips from the previous manufacture. When the new TTCrx chips became available, the TTCPR was redesigned to take advantage of the availability and enhanced features of the new TTCRX(1), and a run of 20 PMC cards was manufactured, and has since been used in integration studies and the testbeam. The TTCPR uses the AMCC 5933(2) to manage the PCI port, an Altera 10K30A(3) to provide all the logic so that the functionality may be easily altered, and provides a 4K deep FIFO to retain TTC data for subsequent DMA through the PCI port. In addition to DMA's which are mastered by the Add On logic, communication through PCI is accomplished via mailboxes, interrupts, and the pass-through feature of the 5933. An interface to the I2C bus of the TTCRX is provided so that internal registers may be accessed, and the card supports reinitialization of the TTCRX from PCI. Software has been developed to support operation of the TTCPR under both LynxOS and Linux.

I. History of the TTCPR

The TTCPR was developed in response to a need for TTC(4) information in the Data Acquisition from TileCal Modules in the ATLAS Test Beam. Specifically, it was desired to have EventID, Bunch Counter, and Trigger Type available from TTC in the data records. It was useful to have the TTC information available to processors in the Data Acquisition crates through PCI ports, and to have the data transferred to the processor's address space via an externally mastered DMA. Accordingly, the TTCPR was designed as a mezzanine card in the PMC form factor. The original cards utilized the older non-radhard version of the TTCRX, because the new radhard version was not available at that time.

When it became clear that the new TTCRX would be available soon and also that it would not be possible to obtain any more of the older TTCRX chips, the TTCPR was redesigned, and enhancements were added to take advantage of the features of the new TTCRX. This new TTCPR was produced and has been used successfully in data acquisition at the ATLAS Test Beam. The card has also been implemented in the PCI form factor. The TTCPR in the PMC version is shown in Figures 1 and 2.

Figure 1. View of TTCPR.

II. Architecture of the TTCPR

A block diagram of the TTCPR is shown in Figure 2. The TTC information is received on a fiber by an optical receiver, amplified, and passed to the TTCRX. The TTCRX uses an on-board serial prom for initialization. All external signals available to the user from the TTCRX are passed to an Altera 10k30A FPGA, which also configures from an on-board serial prom. The FPGA has the ability to read/write a bank of FIFO which is 4 bytes wide and 8k deep, and for versatility the FPGA writes on a 16-bit bus and reads on a 32-bit bus. The interface to PCI is managed by an AMCC 5933 PCI Controller, and hardware supports both add-on and pass through transfers, and

supports also add-on bus mastering for DMA's. The hardware supports also the ability to interact with the TTCRX registers via the I2C port using passthrough transfers.

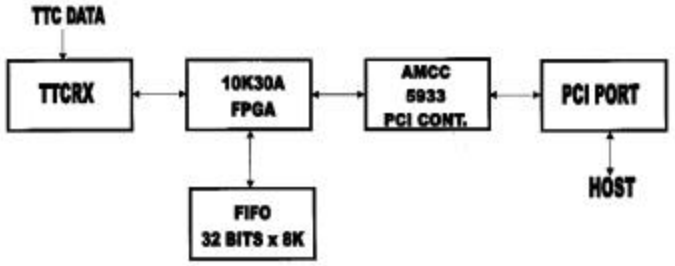

Figure 2: Block Diagram TTCPR.

III. Programming for the TTCPR

The TTCPR has the ability to access to all the TTC information received by the TTCRX. The operation of the TTCPR is governed by the configuration of the on-board FPGA and the user can choose any variation desired by configuring the FPGA. Configuration code for the FPGA is contained in the serial PROM on the card, and for our applications has been generated using the Altera MAX+II software package.

Interaction between the host processor and the TTCPR utilizing the PCI port is through the AMCC 5933 PCI Bridge. The 5933 is initialized from the serial NVRAM, which must be programmed once as described in the AMCC 5933 Guide and contains the PCI vendor and device identification, the configuration space size and type, and other parameters. Data transfers through PCI may use the mailbox registers, the 5933 FIFO's, or the pass-through data path. Software to support operation of the TTCPR in either a polled or interrupt driven mode has been developed in C++ at Argonne. This software has thus far been ported to LynxOS on PowerPC platforms, and to Linux on Intel platforms.

IV. Operation of the TTCPR

Our use of the TTCPR has been to bring TTC information to the data acquisition system for the TileCal setup in the ATLAS test beam. In this application the TTCPR initiates data transfer to a PCI target address specified by the user. The 5933 utilizes Add-on initiated bus mastering to accomplish the transfer. The user supplies an event threshold count and a PCI target address which the Add-on logic in the FPGA stores until the requested number of events has been accumulated in the FIFO, and then initiates the transfer.

In our application the TTCPR buffers the EventID, BCID, and trigger type associated with each L1Accept. These results are made available to the PCI bus when the event threshold count is reached. Interaction between PCI and the Add-on bus is mediated by writing and reading the 5933 mailboxes and registers. Commands such as Reinitialize the TTCRX and Clear Busy, and data such at the Event Threshold and PCI target address for the Add-on mastered DMA are passed by mailboxes. Configuration information and transfer parameters, such as PCI transfer count and Add-on interrupt source are passed by registers.

V. Summary

The TTCPR has been developed by the Argonne group and used to provide TTC information the Data Acquisition system in the TileCal setup in the ATLAS Test Beam. Our objective was to develop a module that could have general application in making available TTC information to processors in the LHC environment. Accordingly the module has access to all TTC information passed to the TTCRX, and may be adapted to transfer any of this information to PCI by reconfiguring the FPGA.

VI. References

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VII. Acknowledgement

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