An Optical Link Interface for the Tile Calorimeter in ATLAS

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Abstract

An optical link interface has been developed in Stockholm for the Atlas Tile-Calorimeter. The link serves as a readout for one entire TileCal drawer, i.e. with up to 48 front-end channels. It also contains a receiver for the distribution of TTC clocks and messages to the full digitizer system. Digitized data is serialized in the digitizer boards and supplied with headers and CRC control fields. Data with this protocol is then sent via G-link to an S-link destination card where it is unpacked and parallelised with a specially developed Altera code. The entire read-out part of the interface has been duplicated for redundancy with two dedicated output fibers. The TTC distribution has also been made redundant by using two receivers (and two input fibers), both capable of distributing the TTC signal. To decrease the sensitivity to radiation, the complexity of the interface has been kept at a minimum. This is also beneficial to the system cost. To facilitate the mechanical installation, the interface has been given an L-shape so that it can be mounted closely on top of one of the digitizer boards without interfering with its components.

I. INTRODUCTION

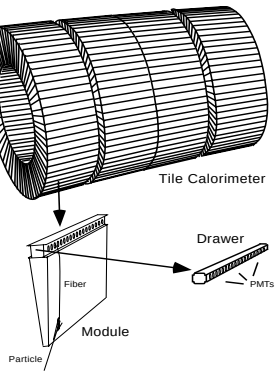

Figure 1: Schematic diagram of the Tile Calorimeter

A. The Tile Calorimeter Digitizer

The Atlas Tile Calorimeter Digitizer [1] digitizes signals from about 10000 PMTs, which record the light generated when particles are absorbed in the calorimeter. The detector electronics is located in "drawers" in the base of each of the 256 calorimeter modules (Fig 1). Each drawer is responsible for reading out 45 PMT channels (32 in the outer calorimeter sections). The PMT channels are digitized by 8 digitizer boards, each capable of reading out 6 channels.

To achieve a high degree of fault tolerance for the readout, the digitizers use Low Voltage Differential Swing, LVDS for the data transmission, and are electrically organized in a star formation, though mechanically mounted sequentially to reduce the number of loose cables (Fig. 2). The 8 boards are mounted so that they are read out from the end towards the middle where the optical read-out interface is located. The boards are connected with purpose designed flat cables made of flexible capton films, "flex foils", in order to provide impedance matched transmission lines.

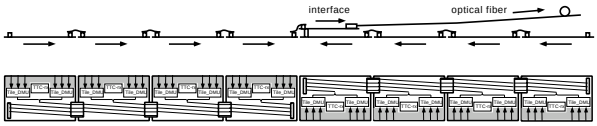

Figure 2: The data flow along a chain of digitizer boards

This, of course, makes the interface a very vulnerable part of the read-out chain.

B. The Optical Link

An optical link read-out interface (Fig. 3) has been designed and tested at Stockholm University. It is designed to fit the over-all design philosophy of the digitizer system as well as the mechanical constraints of the TileCal drawers.

Its task is to read out the data from 8 boards and to receive and distribute TTC signals [2] to the digitizer boards. Each board has 4 serial output lines and one clock input.

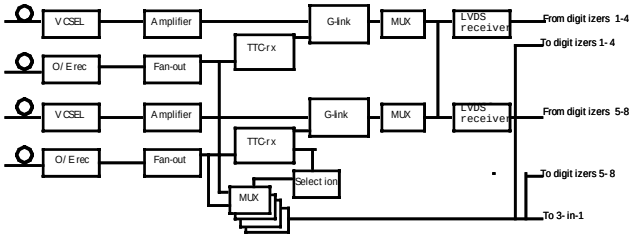

Figure 3: Schematic design of the link

In order to match the fault tolerance it is necessary to avoid single point failure modes in the design. Duplicating the interface board was considered too expensive and not consistent with the space requirements. However, the boards are designed with two parallel systems that operate independently and have

separate fibers for transmission and reception. Both channels transmit continuously, leaving the decision of which channel to use to the link destination card. This design is based on the dual G-link [7] concept developed for the Liquid Argon Calorimeter.

The only functions that are not duplicated are the LVDS receivers, the TTC multiplexers and the decision mechanism that decides which of the two outgoing TTC channels should be transmitted to the digitizers. One error among the LVDS receivers will at worst kill the data from one digitizer board since each receiver serves one board. An error among the TTC multiplexers will at worst kill four boards. For the TTC decision mechanism, the intended solution is to use the PLL lock signal in one of the modules. There are provisions for testing this method in the present design. There will also be a circuit to ensure a long absence of lock before switching. An error in this mechanism will at worst freeze the choice of TTC channel.

II. READOUT

The readout design is intentionally made very simple. The principle is to move the logic components away from the interface card into the receiver card, whenever possible, thus avoiding costly radiation tolerance. The receiver is responsible for all operations on the data content, such as unpacking the data, checking the CRC, choose which channel to use, and reformatting the data for the appropriate application.

The readout uses the HDMP-1032 G-link from Agilent Technologies. This is a 16 bit serial interface for transmission rates up to 1.12 Gbit/s (32 bits at 35 MHz). This corresponds to a transmission rate of 1.4 Gbaud, since the G-link adds 4 encoding bits. The link is presently run at 800 MBaud (20.04 MHz), which is the likely readout speed. However, it may be possible that it will run at 1.6 GBaud (40.08 MHz), which exceeds the specifications, but this has not yet been tested.

The data is first received by 8 LVDS to TTL converters, each chip receiving 4 bits, corresponding to two TileDMUs. This is the only connection between the redundant readout channels, and a failure here will affect both channels. But since there are 8 chips for the LVDS reception, a chip failure will at most affect only two TileDMUs.

The data is then split to both readout channels, where it is multiplexed to the 16 bit input of the G-link. By latching the data on both rising and falling edge, there is no need for a faster clock. The output from the G-link is designed to transmit PECL swings directly into 50 ohm.

The transmission lengths between the TileDMUs and the interface differ from board to board. To synchronize the data, the TTC clocks on each digitizer board is shifted by using the TTCrx [2] clock deskew function.

III. TTC DISTRIBUTION

The interface card is also responsible for distributing the TTC signal to the digitizers. This distribution uses the same concept as the readout. Two channel redundancy with separate receivers and fibers, and a low level of complexity.

The TTC signal received by each channel is first split in four by a 4-port LVDS repeater. One signal for the 3-in-1 system [3], one for the channel's own TTCrx, and two for the digitizers. The latter signals are then split again, also using 4-port LVDS repeaters, two for each channel, for transmission to the 8 digitizer boards. By using the high impedance feature of the repeaters, the transmission lines can be driven by either of the two channels.

For the channel selection, an analog band pass filter with discrete components was first intended, and implemented on the card, but a second solution, using the TTCrx READY signal will also be tested. The READY signal is set when the TTCrx PLL locks on to the incoming signal. With the second solution, channel switching will only occur if the TTCrx cannot establish lock. This solution may also include a delay to avoid unnecessary switching, depending on how robust the TTCrx READY signal is.

IV. IMPLEMENTATION

There are a number of constraints to be considered in the design of the interface card. It has to fit into the drawer, use only 3.3 V and have a low cost.

Since the interface is mounted on top of a digitizer, there is a height limitation. Adding to the limitation are the 6 PMT connectors on the digitizer boards. To be able to mount the interface card directly on top of the digitizer, granting the interface more height, and still have easy access to the PMT connectors, the interface has been given an L shape (Fig. 4). The direct mounting of the card has the added advantage of eliminating one flex foil connection.

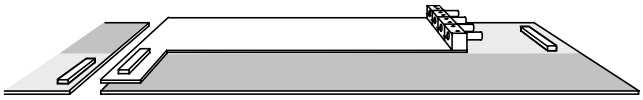

Figure 4: L-shaped card

The disadvantage is that it creates a heat problem, since both the interface card and the digitizer boards have components radiating large amounts of heat, especially the TTCrx and the G-link. To avoid a heat pocket between the boards, the critical components on the interface card are placed on the topside, where they can make better use of the cooling system in the drawer.

A. The platform card

The L shape also creates a problem with the optical transceivers. The shape is too narrow for standard commercial components, and there are no cheap miniature transceivers for 3.3 V, and none at all for 1300 nm reception and 850 nm transmission. To solve this, separate receivers and transmitters have been specially built for the interface, with one end of the card dedicated to the optical communication, with the diodes mounted in ST houses, chosen for size, prize and availability.

Not using integrated components means that the connection between diode/VCSEL and amplifier can be up to 1 cm in length. This is a critical point, for while the circuits on the PCB are matched for impedance, the diode pins are not. To bring the amplifiers closer to the headers, making the diode pins as short as possible, a platform card (Fig. 5) containing the amplifiers, is mounted on top of the interface card. Using a platform card also makes it easier to surface mount the diode pins, greatly improving the impedance match.

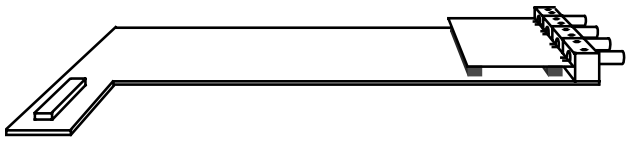

Figure 5: Platform card

B. The transmitter

The transmitter is a standard solution from MAXIM, using the MAX3286 laser amplifier. The MAX 3286/96 series is optimized to drive lasers packaged in standard TO-46 headers, and consequently the VCSEL used, Zarlinks MF444, is packaged in a TO-46 header. This solution is compact and inexpensive.

The G-link output is designed to deliver PECL into 50 ohm. Since the differential MAX 3286 input accepts PECL swings, the connection between these circuits is a straight forward AC coupling with 100 ohm differential termination.

C. The receiver

The receiver is a PIN diode, Zarlink MF432, with a transimpedance amplifier (TIA), Philips TZA3033. Since the connection between the PIN diode and the TIA is critical to the performance, the preferable solution would have been to use a PIN-TIA combination, i.e. a PIN diode with a TIA mounted inside the header. Since there are no PIN-TIAs for this application, the PIN diode and TIA are separate. Since the input current is about 7-8 mA, and obviously very sensitive to noise, special attention has been paid to the layout around the input pin of the TIA. The input capacitance is minimized by surface mounting the diode pins and by removing the power planes beneath the input pins of the TIA.

Also critical to capacitance is the reverse voltage across the diode. Presently the diode uses a reference voltage from the TZA 3033, which is only 2.25 V. Tests will be made with the VCC pin directly connected to the power plane. This will increase the reverse voltage but may introduce too much noise.

The TZA features an automatic gain control loop, AGC, which maintains a stable output at 110 mV for a wide range of input currents. This means that no extra amplification is needed and that the output can be directly fed to the LVDS repeater, using only biased termination for the DC level.

V. THE LINK DESTINATION CARD

The currently used link destination card (LDC) is a single G-link simplex with an S-link output format [4]. This card is only designed for 20.04 MHz operation and can only receive one channel. For full speed testing, a double G-link simplex with 40.08 MHz capacity is needed. Also, it must have a large FPGA, since much of the link data processing has been moved to the destination card. Since there are no commercially available solutions for 40.08 MHz readout, a new destination card would have to be developed if a full speed link is desired. However, if readout speed remains 20.04MHz, the ODIN double G-link destination card [5] could be used, provided that it is fitted with a large enough FPGA.

VI. PROJECT STATUS.

The interface link is presently being used in the testing of the digitizer boards. For these tests, there is no need for the link destination card to have two channel capacity. The operation has been reliable during these production runs, but further tests will be made to determine the optimum performance, including bit error tests and radiation tests.

As of September 2001, a Chicago built interface card is baseline link for TileCal, making the Stockholm interface card an alternative solution. However, a certain development of the Stockholm interface will continue until the Chicago solution is proven. This may include building a version using the CERN developed Gigabit Optical Link (GOL). Such a design would lead to further simplification (eliminating the input multiplexers) better radiation tolerance (the GOL is made in DMILL [6]) and 40 MHz operation.

VII. ACKNOWLEDGEMENTS

We would like to thank Stefan Rydström and Mark Pearce at the Royal Institute of Technology, Section of Experimental Particle Physics, for their help with the design of the transmitter.

VIII. REFERENCES

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