A rad-hard 8-channel 12-bit resolution ADC for slow control applications in the LHC environment

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Abstract

The damage induced by radiation in detector sensors and electronics requires that critical environmental parameters such as leakage currents of the silicon detectors, local temperatures and supply voltages are carefully monitored. For the CMS central tracker, an ASIC, the Detector Control Unit (DCU) has been developed to monitor these quantities in a commercial sub-micron technology. A set of layout design rules guarantees for this device the radiation hardness that is requested for the LHC environment. The key circuit of the DCU is an 8-channel 12-bit resolution ADC. The structure and the performances of this ADC are described in this work.

I. INTRODUCTION

The CMS tracker silicon micro-strip detectors, when exposed to the LHC high levels of radiation, are subject to a number of damaging phenomena. The main effects are an increase of the detector leakage current and a change in the detector depletion voltage. Maintaining the detector integrity and efficiency over their expected 10 years life requires careful monitoring of the detector environmental conditions. A VLSI circuit, the Detector Control Unit (DCU), has been developed for that purpose in the CMS tracker.

The detector hybrid block diagram is shown in Figure 1. The figure represents the global relations between the DCU, the Si micro-strip detectors and the readout chips (the APVs) [1]. The detector leakage currents are monitored using a sensing resistor. This voltage is measured by the DCU Analogue-To-Digital Converter (ADC) and can then be read by the slow control system using the DCU I2C interface [2]. The sensor temperature is measured in two different points using two Negative Temperature Coefficient (NTC) thermistors in parallel. A third NTC thermistor is used to monitor the temperature near the APV ICs. Two temperature and power supply independent currents (20µA and 10µA) are generated inside the DCU and used to drive the thermistors. The APV power supply voltages (2.5V and 1.25V) are monitored by the DCU through two external resistive dividers.

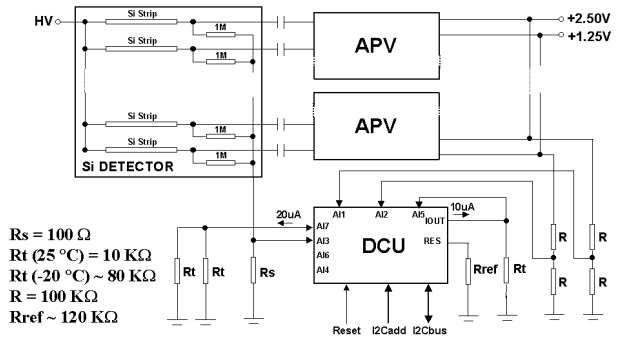

Figure 1: CMS Tracker monitoring system

A single ADC is used inside the DCU to convert the several input voltages using an analogue 8-to-1 multiplexer.

II. DCU DESCRIPTION

The global architecture of the DCU is shown in Figure 2.

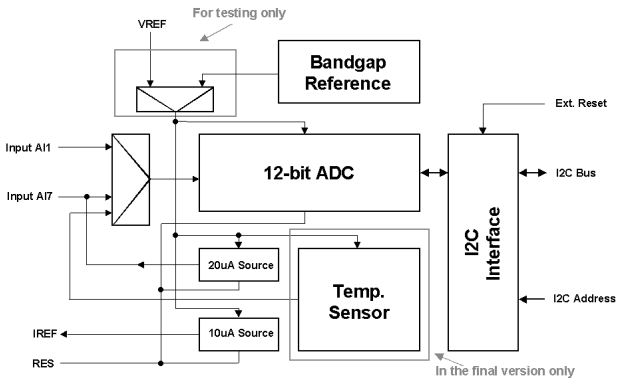

Figure 2: DCU architecture

The DCU is composed of the following blocks: an 8-to-1 analogue multiplexer, a 12-bit ADC, an I2C interface and, a band-gap voltage reference and two temperature and power supply independent current sources. In the final version of the ASIC a diode based integrated temperature sensor has been added. Due to lack of experimental results this last feature will not be described here.

This work will be focused on the operation and performance of the analogue multiplexer and the ADC. The design specifications are summarised in Table 1.

Table 1: DCU Specifications

# of channels	8
Resolution	12 bits
Input Range	GND→1.25V
INL	1 LSB
DNL	1 LSB
Power Dissipation	< 50 mW
Chip Size	< 2mm x 2mm
Conversion Time	< 1 ms

The ADC architecture is of a single slope type [3]. In this type of circuits a constant current charges a capacitor. The resulting voltage "ramp" is compared with the input voltage. A counter is started at the beginning of the conversion cycle and measures the time the capacitor voltage takes to reach the input voltage value. The final count is proportional to the input voltage and represents the conversion result. For the 12-bit ADC described here, the maximum conversion time is 100us (4096 clock cycles at 40MHz).

Two ADC operation modes are possible. In one mode the measurement is made with reference to ground while in the other mode the power supply (2.5V) is taken as the signal reference. These two modes, allow to measure, without loss of linearity, signals that are either close to ground (low input range) or the power supply voltage (high input range).

When operating in the Low Input Range (LIR) mode the ADC integration capacitor is charged from ground until it reaches the signal voltage, while in the High Input Range (HIR) mode the capacitor is discharged from the power supply voltage. Depending on the operation mode A PMOS (LIR mode) or an NMOS (HIR mode) based comparator is used to take advantage from their intrinsic common mode ranges. Both comparators use a two-stage topology with positive feedback.

In order to guarantee high linearity and low thermal sensitivity the ADC integration capacitor was implemented using a metal-to-metal (MIMCAP) 100pF capacitor. However, the non-linear gate capacitance of the input transistors of the two comparators is connected in parallel to the integration capacitor degrading the global non-linearity of the ADC. To limit the effect of this non-linear component of the total capacitance, the size of the input transistors has been chosen to be as small as possible. However, small devices result in large comparator offsets. To circumvent this problem, the following offset cancellation scheme has been implemented: for each data acquisition, two ADC conversions are performed with the capacitor and the input voltages connected to alternative inputs of the comparator as shown in Figure 3. The average of these two measurements is taken as the true result of the measurement. The offset is cancelled because in the two consecutive measurements it appears with opposite signs.

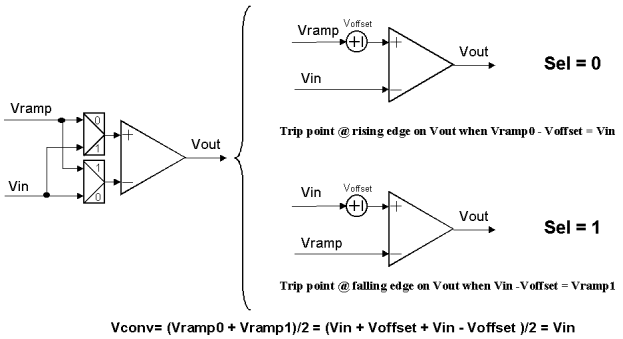

Figure 3: automatic offset cancellation

The IC interfaces with the tracker control system through an I2C bus. This is used to start the acquisitions, to select the input channel and the operating mode and to read the results.

The digital part of the chip uses triple redundancy to insure protection against SEU effects.

The global layout of the DCU is shown in Figure 4 where the analogue core of the ADC, the digital blocks and the band-gap voltage reference are put in evidence.

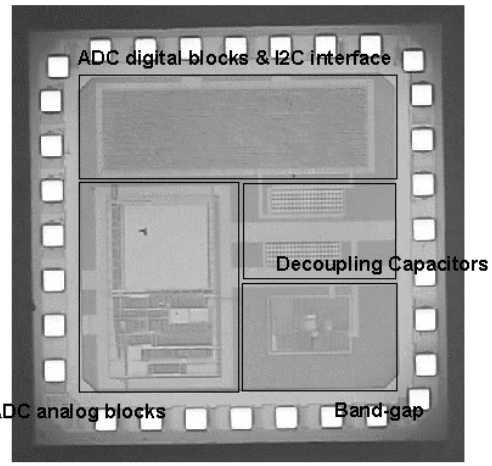

Figure 4: DCU layout

III. TEST RESULTS

A custom test-board for the DCU A/D converter prototype has been developed. It is based on a commercial micro-controller (Microchip PIC16F877) which interfaces via an I2C link the device under test (DUT) and a 20-bit resolution D/A converter used to generate the input voltages for the DUT. Two 16-bit resolution A/D converters are used as measurement references, one for the LIR mode and the other for the HIR mode. The micro-controller is connected to a host PC via a standard RS232 interface. A schematic block diagram of the test-board and a picture of the whole test-setup are shown in Figure 5 and in Figure 6, respectively.

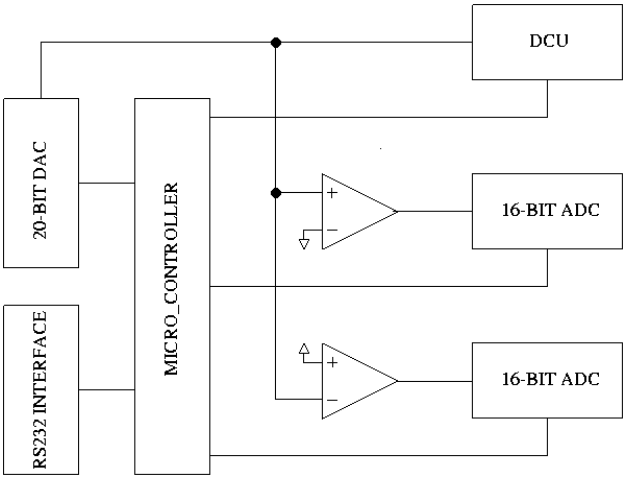

Figure 5: DCU test-board block diagram

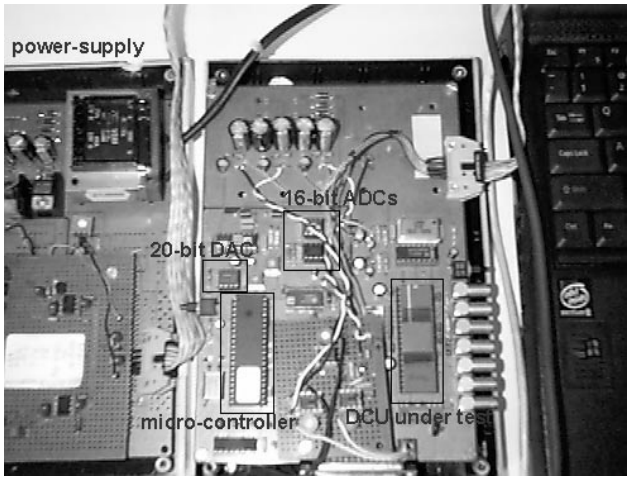

Figure 6: DCU test setup

All the digital functions of the IC have been successfully tested.

The A/D converter parameters like gain, Integral Non-Linearity (INL), Differential Non-Linearity (DNL) and Transition Noise (TN) RMS, have been measured for the two operating modes on all of the input channels. The evaluation and characterisation tests were automated using specific test programs running in the micro-controller. The test results were read from the micro controlled after completion via the RS232 interface.

A sequence of 128 input voltages has been applied in the two input ranges GND→1.25V in the LIR mode and 1.25V→VDD in the HIR mode. In both operating modes the gain is between 2.18 and 2.20 LSB/mV corresponding to a resolution of 500uV/LSB.

Figure 7 shows the A/D INL for input voltages in the 0 to 1.25V range (LIR). The periodic "saw-tooth" shape observed in the picture reveals no intrinsic ADC non-linearity over this range, where the INL is less than 1 LSB according to the specifications. If the extended range, 0 to 2.5 V, is taken, the non-linearity due to limited common mode range of the comparator is revealed as can be seen from Figure 8

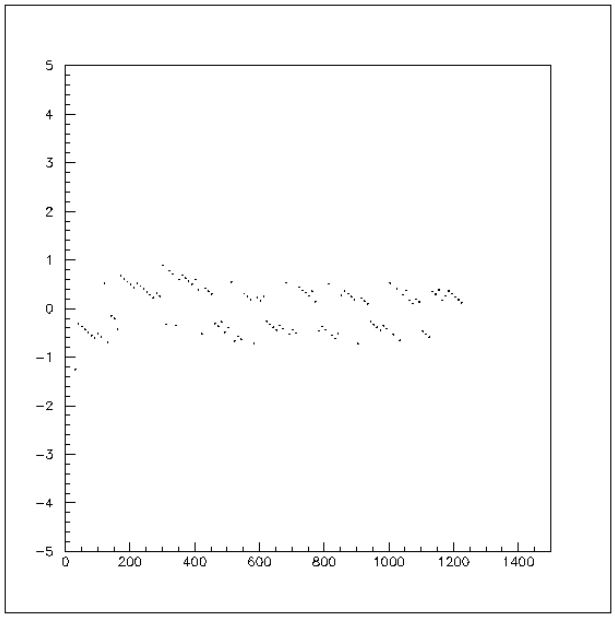

Figure 7: ADC INL in the LIR mode (input range = GND→1.25V)

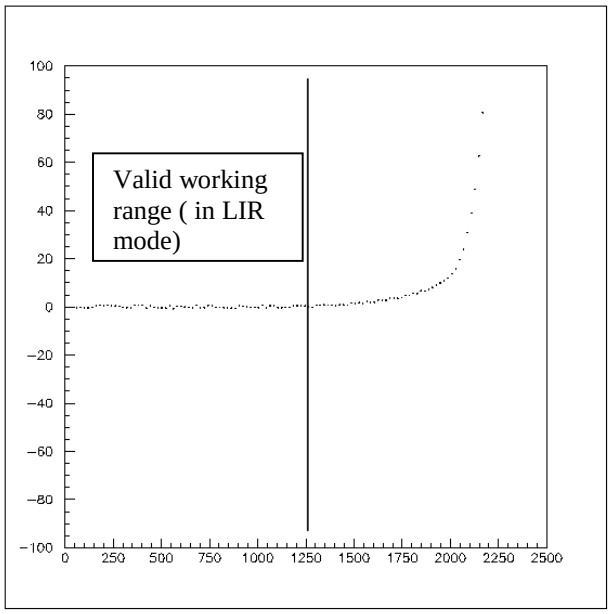

Figure 8: ADC INL in the LIR mode (input range = GND→VDD)

The differential (Figure 9) non-linearity has been evaluated and reveals a monotonic A/D converter characteristic and no missing codes.

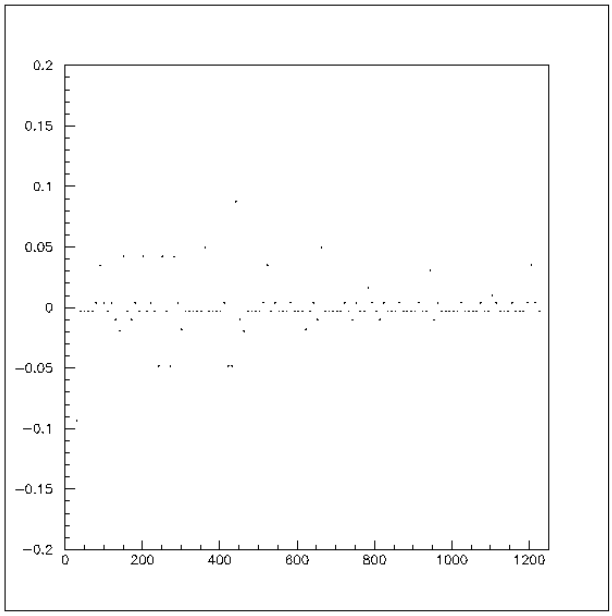

Figure 9: ADC DNL in the LIR mode (input range = GND→1.25V)

Finally, 1024 samples of a fixed voltage were taken to evaluate the internal A/D noise (transition noise). From Figure 10 it can be concluded that the transition noise has an RMS value smaller than one LSB. The RMS of the transition noise can be evaluated applying a sequence of very small voltage steps to the ADC input and evaluating the steepness of the transition between two adjacent ADC outputs. This analysis leads to an noise RMS around 0.25 LSB.

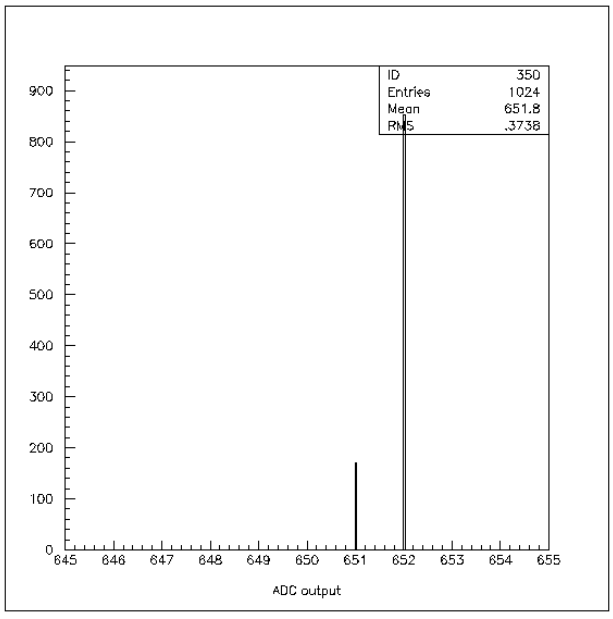

Figure 10: ADC output distribution for a fixed input voltage

Power dissipation has been evaluated: with the ADC working at the maximum acquisition rate: the absorbed power is less than 40mW. A preliminary ADC temperature characterisation shows no significant changes in ADC performance with temperature.

Several samples of the A/D converter have been irradiated with X-rays up to 10 Mrad (dose rate 25 Krad/min). No changes in the INL and in the transition noise have been observed. A gain decrease of 0.4% / Mrad with the irradiation dose has been measured (see Figure 11).

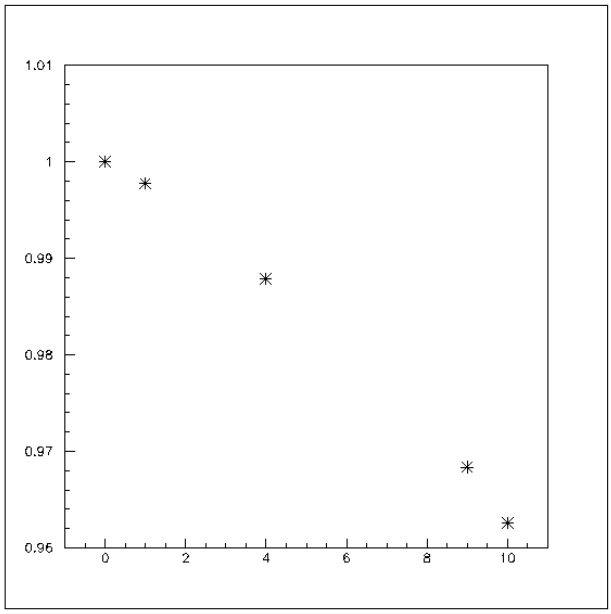

Figure 11 : A/D converter gain as a function of the dose

IV. SUMMARY

As part of the CMS tracker slow control system, a mixed-mode ASIC has been developed to monitor the detector leakage currents, temperatures and power supply voltages. The IC has been implemented in a commercial sub-micron technology using a special set of layout design rules to guarantee the level of radiation tolerance required in the LHC environment. The main building block of this IC is a 12-bit ADC whose characteristics have been described in this work. The ASIC has been irradiated with X-rays up to 10 Mrad with only minor changes in the circuit performance.

A second version of the IC including an integrated temperature sensor has now been submitted for fabrication

V. REFERENCES

[1] CMS Technical Design Report, CERN/LHCC/98-6 (1998)

[2] I2C Bus Specification, Signetics (1992)

[3] B.Razhavi, Principles of Data Conversion System Design, IEEE Press (1995)