The Muon Detector FE Trigger Electronics

A. Balla, M. Carletti, M. Beretta, P. Ciambrone, G. Corradi, G. Felici

INFN - Laboratori Nazionali di Frascati - Via E. Fermi 40, 00044 Frascati (Rome), Italy
Giulietto.Felici@lnf.infn.it

M. Gatta

INFN – Roma2 - Via della Ricerca Scientifica 1, 00133 Rome, Italy

Abstract

The first stage of the muon trigger electronic system for the LHCb experiment will be described. The LHCb muon trigger [1][2] has been designed to detect muon tracks with large transverse momentum and the architecture relays on 1248 *Trigger Sectors* (TS) built by the first stage of the electronic chain.

About 120,000 *physical channels* are firstly merged to generate ~ 26,000 *logical channels* both in the chambers front-end and in the *Intermediate Board* (IB) system. Then in the *Off Detector Electronics* (ODE) boards, the logical channels are synchronized to the bunch crossing, arranged to implement the required *trigger sectors*, and, finally, sent to the *Level-0* (L0) trigger logic through 1248 optical links at 1.6 Gbit/s.

The ODE board provides also a measure of the signal arrival times with a 1.5 ns time resolution and implements the L0-pipelines, the DAQ interface via a 1.6 Gbit/s optical link and the ECS interface.

I. Introduction

The LHCb muon spectrometer [1] is made of five stations (M1 – M5) and each station has two detector layers with independent readout. Each layer of M2 – M5 stations is made of two different gaps with hardware OR-ed readout. Then ORs from each layer are logically OR-ed on *Front-End* (FE) boards to ensure high detection efficiency (99%) and redundancy. Furthermore each station is subdivided in four regions with different logic pad dimensions

Considering the readout [3][4], the LHCb muon detector is made of 126832 FE *physical channels*, while the muon trigger is based on 28224 *logical channels*. *Logical channels* are built starting from FE board outputs and, for some chambers and/or regions, they correspond to the FE board outputs

On the other hand, because single channel occupancy and electrode capacitance (a big capacitance means big noise and long readout time), for some stations and/or regions the readout electrodes have been segmented. Then some additional electronics is required to build up *logical channels*. That intermediate stage is called *Intermediate Board* system [5] and is made of about 160 boards. Each IB board can manage up to 192 LVDS input signals and 60 LVDS output signals.

The following stage, the *Off Detector Electronics* boards, receives the 28224 *logical channels*, both from FE and IB system, synchronizes incoming signals to the bunch crossing and sends them to the trigger system via high throughput (1.6 Gbit/s) optical links. Each board can manage up to 192 input LVDS signals and 12 output optical links.

The ODE board includes *Level-0* trigger logic as well. Formatted data from L0 derandomizer are sent to the experiment DAQ through a (further) dedicated optical link. Besides, data from M2-M4 are foreseen to be used in the *Level-1* trigger logic. A CAN interface manages the communications with the experiment ECS.

Because the huge number of input channels per boards (192 LVDS) and the very strict requirements on timing performances for optical link connections (less than 100 ps *peak to peak* on clock jitter) the design of this board has been very challenging. Over 140 boards will be used to fully instrument the muon detector

Finally, as both IB and ODE systems are localized close to the detector to minimize the cables length, both board types must be implemented using radiation tolerant components

II. The IB System

A. The IB Board

The most elementary part of the LHCb muon trigger system is build by the ODE board and is defined as *Trigger Sector*. The ODE board generates TS starting from the *logic channels*. As said before for some stations and/or regions *logic channels* correspond to the FE (DIALOG chip [6]) outputs; for example all the FE outputs of station M1 correspond to *logical channels* (Table 1 shows the number of front-end channels per station and region)

Table 1: FE boards/channels per station/region

Station	Region[#]	Number of chambers	FE boards x chamber	FE channels x board	FE channels x chamber
M1	R4	192	3	4	12
	R3	48	12	4	48
	R2	24	24	4	96
	R1	12	24	8	192
M2/M3	R4	192	3	8	24
	R3	48	12	8	96
	R2	24	8(P)/6(W)*	2(P)/8(W)*	16(P)/48(W)*
	R1	12	14	8	112
M4/M5	R4	192	3	2	6
	R3	48	6	4	24
	R2	24	6	8	48
	R1	12	12	8	96

[#]R1(4) = Inner (outer) region; * P= PAD readout W = Wire readout

On the other hand, some regions of stations M2-M5 require a combination of several FE outputs coming either from the same chamber or from different chambers to build up *logical channels*. An example is given in Figure 1: a logical vertical channel is made of 4 FE channels belonging to two different chambers, while the horizontal one is made of 24 FE channels belonging to the same chamber. The electronics used to build up *logical channels* is referred as *Intermediate Boards* system

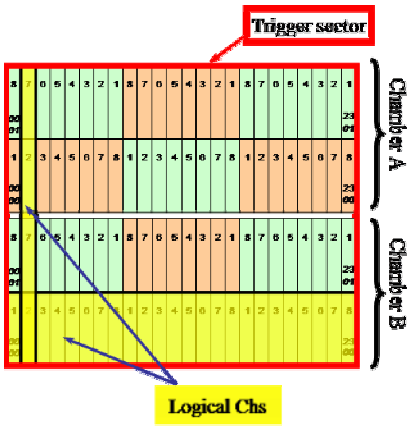

Figure 1: M2/M3-R3 Trigger sector and logic channels structure

The IB system has to manage ~ 8600 LVDS links. To reduce the number of boards each IB must have a considerable number of input/output signals. Moreover, to avoid efficiency reduction, FE signals skews should be minimized. Finally, as the system has to work close to the detector to minimize cables length, radiation tolerant components must be used in the board.

The design of the IB board had the following constraints:

- manage a huge number of input/output connections;
- minimize the number of boards required to match the detector topology;
- minimize the input/output signals skew;
- use components able to work up to an integrated dose of 10 krad.

The IB board input/output modularity has been chosen using the Table 2 (the table gives, for each station and region, the number of FE outputs together with the correspondent *logic channels* involved in a TS) and assuming ~ 520 contacts available for I/O connections (that is about the number of connections available on the long edge of a 6U VME board with PCI connectors).

Table 2: FE outputs and *logic channels* for TS

	M1	M2	M3	M4	M5
R1					
R2				48/28	48/28
R3		96/28	96/28	24/10	24/10
R4		96/28	96/28	24/10	24/10

According to the Table 2, 192 inputs match most of the detector topology. Then 192 pairs have been chosen as IB input modularity and, as a consequence, 60 pairs as IB output.

To minimize the number of boards (because the chamber/TS geometries we have 5 different IB I/O configurations) the logic functions have been implemented using programmable devices. That choice allowed us to design a single PCB to fit the whole detector geometry.

The use of anti-fuse technology for programmable devices (we have used ACTEL devices) gives also an intrinsic robustness in moderate radiation environment (like the levels foreseen near the LHCb detector).

Finally, a big effort was devoted to match the *skew* requirements, due to the huge number of I/O managed by the board. In fact, though the PCB design was optimized using a symmetric structure both for components placement and signal path routing, the main source of skew came from the FPGA itself, due to the poor resources to control the signal transit time. The final design uses a tree structure that is spanned over three FPGA as shown in Figure 2.

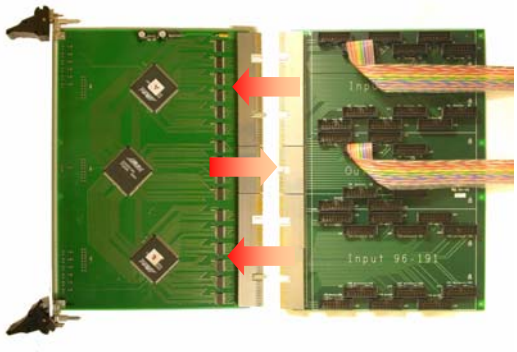

Figure 2: IB (left) and TB (right) prototypes

B. Signal Skew simulation and measurements

As PCB trace delay is well known we concentrate our efforts on the simulation of the FPGA to minimize the signal time skews. Figure 3 shows the results for M2/M3-R3 chambers (that is the worst case of chambers/TS configuration concerning the I/O signal skews), while Figure 4 shows the skews measured on the IB first prototype. Only 96 out of 192 signals are shown as the board is made of two identical sections.

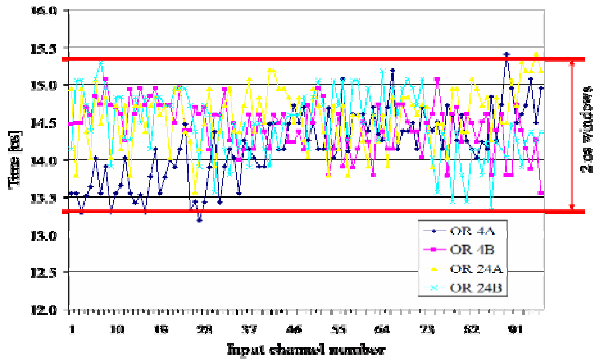

Figure 3: Output signal skews (FPGA simulation)

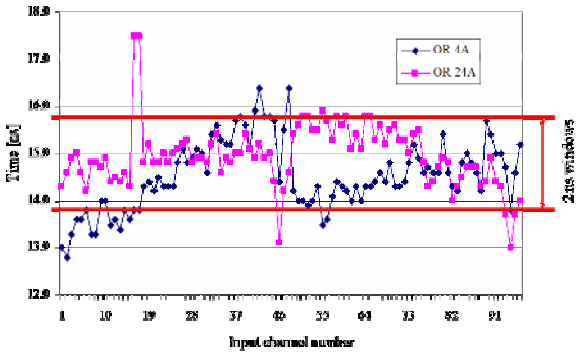

Figure 4: Output signal skews (board measurements)

Measurements show that most of the signals are inside a 2 ns window, (the single channel out of window was due to a failure in one LVDS receiver).

C. The TB Board

IB board uses very high-density connectors, while FE board modularity ranges from 4 to 8 (as shown in Table 1). Then a passive *transition board* (TB) (Figure 2) has been designed to accommodate all chamber geometries

Both IB and TB boards are located in a mechanical standard 6U VME crate with custom backplane. The backplane allows to interconnect IB and TB boards and to distribute low voltage (+ 2.5V and + 3.3V) to the IB boards. The crate can hold up to 16 boards (5 slots have been reserved for crate power supply).

III. OFF DETECTOR ELECTRONICS

The ODE board implements the L0 stages of muon front-end electronics [7]. The board decodes and manages the TTC system signals, receives and synchronizes the *logical channels*, implements the L0 buffer and L0 derandomizer, integrates the L0 trigger logic, DAQ and ECS interfaces. A block diagram is shown in Figure 5

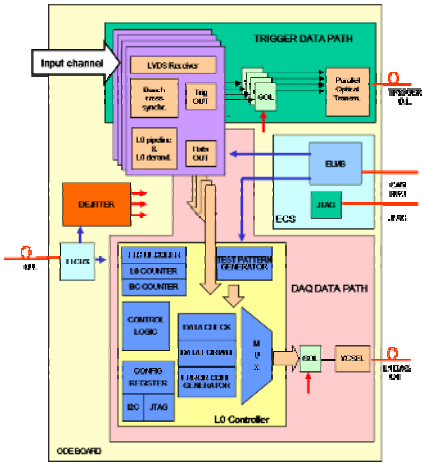

Figure 5: ODE board block diagram

The board receives up to 192 *logical channel* signals in LVDS standard and merges them in (up to) 12 TS to be sent to L0 trigger systems via high rate optical transmitters.

The arrival time of incoming signals, respect to the master clock phase, is also measured and sent as a formatted frame to L1 DAQ boards.

An ELMB [8] board with a CAN interface is used to communicate with ECS while an internal I^2C bus is used to control the board registers and setting.

Test facilities have been implemented to improve maintenance and debug, allowing remote diagnosis, error condition detection and system operation monitoring.

A *board controller* manages most of the previous ODE operations. It has been implemented in an anti-fuse technology FPGA using triple redundancy technique to increase SEU immunity. The first board prototype is shown in Figure 6

Figure 6: ODE prototype

As in the IB system, a passive *transition board* (TB) is used to accommodate different topology of input *logical channels*. The ODE board and TB are 6U wide and they use the same crate of the IB system.

A. TTCrx and clock

The ODE board must be a completely synchronous machine with the bunch-crossing clock (40.08 MHz).

The board receives the master clock and synchronization signals, delivered by TTC system [9], via optical link and TTCrx chip.

To be compatible with the GOL high-speed serializer specification [10], a narrow bandwidth PLL is used to reduce the jitter of recovered clock (~ 240 ps *peak to peak*) to about 40 ps. The de-jittered clock is then distributed to all chips on the board using a tree distribution with a maximum *peak to peak* jitter of 100 ps.

TTC commands (*L0_yes*, *BC_res*, *EV_res*, *L0_res*) are decoded by the *board controller* and synchronously re-distributed on the board.

B. SYNC Chip

Input stages, L0 pipelines and TDCs have been implemented in a custom rad-hard chip (SYNC [11]) as shown in Figure 7.

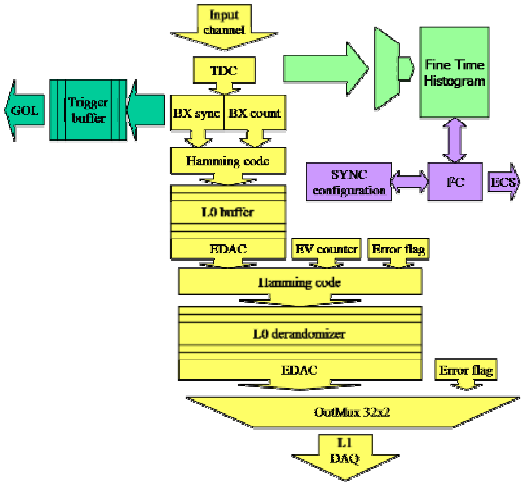

Figure 7: SYNC chip block diagram

The SYNC chip can manage 8 LVDS input signals. Incoming data are synchronized to bunch crossing clock and tagged with a bunch identifier number (*BX_cnt*).

The synchronized hits (8 bits) and the LSB of *BX_cnt* (2 bits) are available, at the rate of 40 MHz, on the chip output to be arranged in TS.

The arrival time of the input signal within the master clock period is also measured using a 4-bits TDC with a resolution of ~1.5 ns.

Both TDC data and bunch identifier are hamming coded and stored in the L0 buffer until a L0 decision arrives.

For each L0 trigger (*L0_yes*) data are extracted from the L0 buffer and pushed toward the L0 derandomizer (together with error flags and event counter identifier) where they can be read by the *board controller*.

Some facilities have been implemented in the chip:

- pseudo-random or predefined pattern can be sent to trigger or DAQ system to verify link integrity;
- internal histogram memory can be activated for fast time calibration and detector time alignment;
- channel mask can be applied to input channels.

C. Trigger Data Path

The ODE trigger interface allows a unidirectional data transfer to muon trigger system at 40.08 MHz.

The input logical channels belonging to same TS must be merged in a single data frame, tagged with the right bunch crossing identifier and sent to the muon trigger processing board.

Therefore output signals of several SYNC chips must be collected together to assemble a TS data. Due to the different chamber topology the number of SYNC chips required to implement TS can be 2, 3 or 4, as shown in Table 3.

Table 3: SYNC and active channels per station/region

Station	Region	Logical channels x TS	SYNC x TS	Active channels x SYNC	TS x ODE	Active ODE channels
M1	R1 R2 R3 R4	24	3	8	8	192
M2/M3	R1 R2 R3 R4	28 16 28 28	4 2 4 4	7 8 7 7	6 12 6 6	168 192 168 168
M4/M5	R1 R2 R3 R4	24 14 10 10	3 2 2 2	8 7 5 5	8 12 12 12	192 168 120 120

To fit all configurations and to minimize the number of ODE boards, the SYNC chips have been mounted on three different types of piggy board housing 2, 3 or 4 chips. All possible TS topologies are obtained with an appropriate combination of piggy board types on a single ODE motherboard. This architecture does not use the ODE 192 inputs for all stations/regions, but this drawback is largely compensated by using a single ODE board PCB for the whole detector.

The SYNC outputs belonging to the same piggy board are merged in a single 32 bits data frame and sent to the GOL serializer. The frame (see Figure 8) contains up to 28 bits of

data hits, 2 bits of *BX_cnt* and 2 *switch bits* to ensure data alignment in the trigger system.

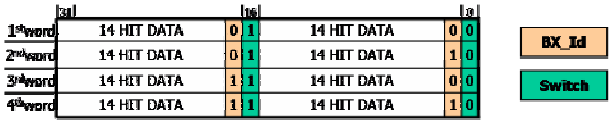

Figure 8: Trigger data frame

Serialized data from different GOLs are sent to the trigger system using a 12 channels parallel optical link (1.6 Gbit/s each). Again, due to the used architecture for some stations/regions not all 12 links are active.

The main advantages of optical links with respect to standard copper links are:

- high reliability for data transfer over 100 m;
- electrical isolation (no ground loops and common mode problems);
- high data throughput.

Besides, using a parallel device that integrates 12 optical links in a single component, allows high aggregate data bandwidth without increasing number of devices and costs.

The GOL chip is used in Ethernet mode with 8B/10B coding.

D. DAQ Data Path

Valid data are retrieved from SYNC L0 derandomizer by the *board controller* at the rate of the *L0_yes* signal (average rate ~ 1 MHz).

Each SYNC chip produces a *dataword* (32 bits) of TDC data and an *infoword* (32 bits) containing bunch counter identifier, event counter identifier and error flags. These two words are multiplexed on a 32 bits wide output bus. Therefore two accesses are required to read complete SYNC information.

The *board controller* reads two SYNC chip at the same time to match the L0 read-out time specification (900 ns).

The DAQ data frame is prepared with the *dataword* and temporally stored in an internal FIFO. The *infoword* is used to verify board alignment and data corruption and to create the footer frame. At the end of the SYNC read-out process a frame header is created containing the bunch counter and the event counter information. Then the complete data frame is serialized by a GOL chip, driving a VCSEL laser diode, and sent to L1 DAQ board.

IV. CONCLUSIONS

The architecture of the muon front-end trigger electronics has been shown and the adopted solutions to fulfil the experiment requirements have been presented.

A high detector granularity (~126000 channels) has been adopted because noise and rate constraints. Then an intermediate stage (the IB boards) has been introduced to build up logical channels, as the trigger system requires coarser detector read-out segmentation

The use of programmable devices, together with the use of a *transition board* allowed fitting the whole detector with a single PCB layout. Efforts have been devoted to minimize the output signal time skews.

Logical channels are synchronized and merged in Trigger Sectors (TS) in the ODE boards. Parallel optical links (1248 channels) are used to send data to the trigger system at 1.6 Gbit/s. The ODE board integrates L0 front-end electronics as well. A single ODE motherboard and three types of piggy board are used to match all TS topology.

V. REFERENCES

[1] *Muon system technical design report*, LHCb TDR 4;

[2] E. Aslanides et al., *A synchronous architecture for the L0 muon trigger*, LHCb note, LHCb-2001-010

[3] A. Lai et al., *Muon detector front-end architecture*, LHCb note, LHCb-2000-017

[4] A. Lai et al., *Muon Detector Front-end Architecture: an update*, LHCb note, LHCb-2001-030

[5] A. Balla et al., *Muon Off-Detector electronics: The IB system*, LHCb note, LHCb 2003-023

[6] S. Cadeddu, A. Lai, *DIALOG: a chip for the muon detector front-end and logic*, LHCb note, LHCb-2001-062

[7] J. Christiansen, *Requirements to the L0 front-end electronics*, LHCb note, LHCb-2001-014

[8] Technical documentation on the ELMB can be found at URL: http://atlas.web.cern.ch/Atlas/GROUPS/DAQTRIG/DCS/LMB/SB/index.html

[9] R. Jacobsson, B. Jost, *Timing and fast control*, LHCb note, LHCb-2001-016

[10] *Gol reference manual, Gigabit optical link transmitter* manual, CERN-EP/MIC version 1.3 May 2002

[11] S. Cadeddu et al., *The SYNC chip in the Off-Detector Electronics of the LHCb muon system*, LHCb note, LHCb-2001-063