Facilitated design kit development for analog IC elaboration on semicustom array A 3201.

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Abstract

The results of a further evolution of the bipolar application specific semicustom array (ASSA), intended for designing prototype ICs, used in physical experiments, are described. That is achieved by PC platform adaptation of the IC developer's Design Kit on this array, by using thoroughly tuned SPICE-models, reflecting the temperature dependences over the chip, when it works, and the statistical dispersions arising during the production and so on.

The development time frames can be significantly reduced due to the fact that an engineer should merely design the schematics and order the topology of connections in ASSA, that is to be made by a technological company. Thus, the usage of Facilitated Design Kit, consisting of models simplified in comparison with widely known CADs, allows a significant reduction of the time frame of prototype IC development. Subsequent ways to improve the bipolar application specific semicustom array and its elements are considered.

I. DESIGN KIT DEVELOPMENT

A. Approach

The results of works connected with the creation, production and improvement of a bipolar analog application specific semicustom array, intended for use in physical experiments, were shown in [1]. The array consists of eight channels for data acquisition and signal preprocessing from multichannel detectors with capacitances up to 100 pF.

During prototyping it is very important to minimize the cost and time frames for the development and production of ICs along with providing the given technical parameters. To reduce the time frames of prototyping (as required by the earliest stages of large physical experiments at LHC) it is important to conduct simulations on the PC platform by the popular pSPICE (OrCAD) products. Instead of the well-known and quite expensive CADs, that use the modern Design Kits, the pSPICE simulation was found to be quite enough during prototyping. By using ASSA, as a set of components already made on the chip, one needs to order merely the design of the topology of the final plating to connect the elements. Thus, we can significantly reduce the time frames as well. Consequently the prototype IC development project consists of two important stages: first, simulations on PC using the suggested thoroughly tuned SPICE-models in OrCAD (for example); second stage is linked with topology designing and IC production. Production company ("PULSAR") accounts for the second stage. Taking into consideration the low cost of manpower in Russia, the topology development can be provided within the sums assigned for IC manufacture. Typically the time frame of prototype IC development and manufacture does not exceed 3 months from the moment of receiving the accurate definition of specifications without significant rise in prices.

The prototyping process using the design kit is schematically shown in Fig. 1. The work is conducted in a close collaboration of the customer (Physical Experimenter) and the engineer (IC Designer). On receipt of the Specifications, the IC Designer carries out a series of simulations with PC (pSpice simulations). The engineer uses the Design Kit, in which all the models under all possible conditions are provided. The engineer is required only to elaborate the circuit and conduct the necessary simulations, what occupies a minimal time. That results in Schematics, which is passed on to the technological company. Further follows the process, for which the company is responsible. There the layout files are prepared, containing all necessary mask patterns. Then the Layout Versus Schematics (LVS) and parasitics verifications are made. The time, needed to manufacture the chip, is reduced to a minimum, since we use a semicustom array, especially the application specific one. In this case the customer should order merely one or two metal plating layers. After manufacturing the semicustom ICs undergo tests both on wafer and after encapsulation. The test results are used to extend the Database on the elements of semicustom array, on the basis of which the Spice models are more accurately verified.

B. PSpice model verification

The application specific semicustom array (ASSA) is made by bipolar technology with $f_t \geq 5$GHz. In order to obtain more reliable simulation results the SPICE-models of certain ASSA components were refined. In particular: the temperature coefficients of the base-emitter junction, Zener

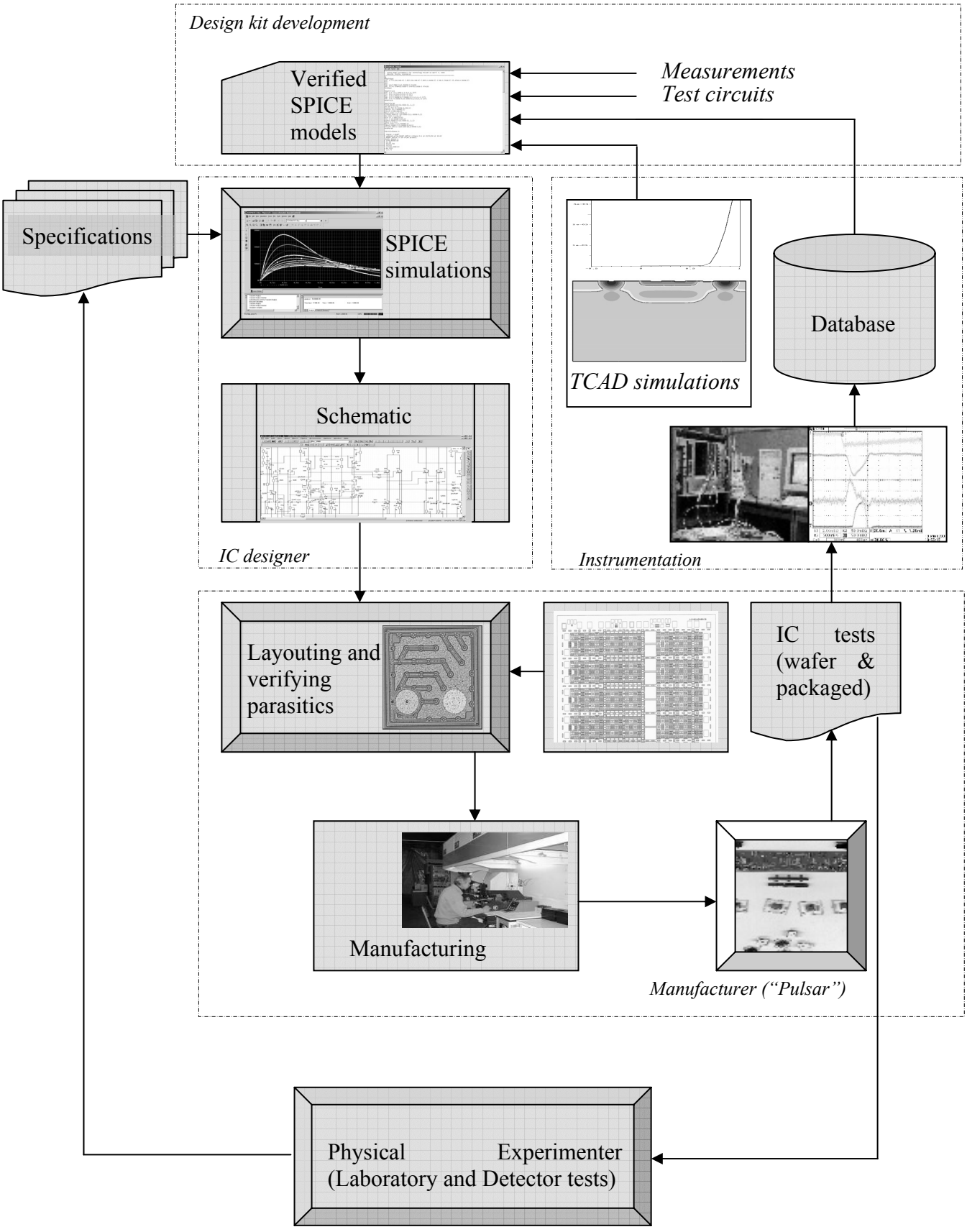

Fig. 1. Prototyping process

diodes and resistors. The spread of stabilization voltages and noise of Zener diodes was studied as a function of bias current. By using the refined models there were verified the static, dynamic and noise characteristics of ASSA components. The measured parameters are partially adduced in table 1.

Table1

Parameter	ΔI_1 (10…600 μA)	ΔI_2 (600…1000 μA)	ΔI_3 (1..1,6 mA)	ΔT_1 (20..70°C)	ΔT_2 (70..130°C)
$\Delta U_{be\ 2x6}$, mV	322	21	40	-80 (I=820μA)	-73 (I=820μA)
$\Delta U_{be\ isogr}$, mV	0,5	5	30	–	–
$\Delta U_{be\ 2x18}$, mV	38	25	96	–	–
ΔU_{stab}, V	0,85	0,18	0,14	0,05 (I=600μA)	0,06 (I=820μA)
ΔR_{HR}, kOhm	–	–	–	0,48 (12%)	0,39 (9%)
ΔR_{LR}, Ohm	–	–	–	-32 (6%)	6 (1%)

In the first column there are enumerated the following parameters:

$\Delta U_{be\ 2x6}$ - spread or change of base-emitter voltage of transistors of the size 2x6 μm sq.

$\Delta U_{be\ isogr}$ - spread or change of base-emitter voltage of the isogradient transistor pair

$\Delta U_{be\ 2x18}$ - spread or change of base-emitter voltage of transistors of the size 2x18 μm sq.

ΔU_{stab} – spread or change of the stabilization voltage of Zener diodes

ΔR_{HR} – change of resistance of a high-ohmic resistor

ΔR_{LR} - change of resistance of a low-ohmic resistor

The second, third and fourth columns contain the results of measuring the spread of parameters (in a batch of samples) in three sub-ranges of working currents.

The fifth and sixth columns present the change of parameters for two temperature ranges at fixed bias currents.

It follows from the table data, that a partial temperature compensation of the Zener diode's change in stabilization voltage is possible due to the base-emitter junction of a transistor, connected in a follower configuration. Obviously, the temperature coefficients of low-ohmic and high-ohmic resistors in the temperature range of (0…70)°C have close and opposite sign values and therefore can be employed to create thermo-stable potentials. Besides, the data, presented in table 1, allow to make a conclusion on the optimality of transistor currents in the range of (600…1000) μA and Zener diode currents in the range of (600…1600) μA.

At present two units have been made on this array: analog chip with 8 preamplifiers-shapers and analog-digital one, containing 8 voltage comparators, output drivers and common "OR" block. [2] By T-CAD simulation the element size reduction down to sub-μ dimensions was researched. The reproducibility of the technology process was getting worse with reduction of element size. Moreover, that reduction essentially affects the parameters of electronic devices (operational amplifiers, comparators etc.) [3], temperature dependences, within-chip and from-chip-to-chip statistical dispersions. AC parameters were researched by special test structures, that had been manufactured on the basis of ASSA.

II. Conclusion

Thus, an approach to the development of the prototype ICs has been elaborated, being distinguished by shortened times of design and production. In the capacity of a basis for development there was chosen the application specific semicustom array A3201, presented earlier [1].

III. References

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