Sector Logic Implementation for the ATLAS Endcap Level-1 Muon Trigger

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Abstract

We present development of the Sector Logic for the ATLAS endcap Level-1 (LVL1) muon trigger. The muon tracks from the interaction point (IP) are bent by the magnetic fields induced by the ATLAS toroidal magnets. The Sector Logic reconstructs three dimensional muon tracks with six levels of transverse momentum (pT) by combining two sets (R-Z and ϕ-Z) of information from the Thin Gap Chamber (TGC) detectors. Then, it selects two highest pT tracks in each trigger sector.

The Sector Logic module is designed in pipelined structure to achieve no-dead-time operation and shorter latency. Look-Up-Tables (LUTs) are used so that any pT threshold level can be set. To achieve these, we adopted SRAM embedded type FPGA devices. The design and its performance are given in this presentation.

I. The ATLAS Level-1 Trigger System

A. Overview of the ATLAS Level-1 Trigger System

The ATLAS trigger and data-acquisition system consists of three stages of online data reduction. The LVL1 trigger system [1] is its first stage. It receives event data at the rate of around 1GHz at 40.08MHz bunch-crossing rate, and has to reduce the selected-event rate down to 75kHz within 2.5μs. The ATLAS LVL1 trigger system consists of the Central Trigger Processor (CTP) and two detector-specific sub-systems: Calorimeter Trigger and Muon Trigger. The muon trigger sub-system employs two kinds of trigger chambers: TGC for the endcap region and Resistive Plate Chamber (RPC) for the barrel region. The Muon Central Trigger Processor Interface (MUCTPI) combines outputs from both systems and sends them to the CTP.

B. TGC Layout and its Trigger Scheme

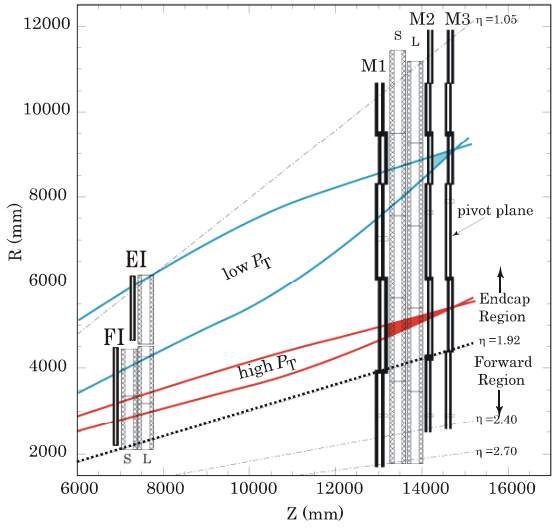

Figure 1: TGC Layout and its trigger scheme.

Figure 1 is a longitudinal side view of TGC layout. The TGCs cover a pseudorapidity range $1.05 < |\eta| < 2.70$. The TGCs are arranged in seven layers in each side: one triplet (M1) and two doublets (M2, M3). Each layer gives hit data in

both R and ϕ coordinates. A muon track is bent by the magnetic field of toroid before reaching TGC triplet. The information on its charge and pT can be calculated from the measured deviation from projected straight line towards the IP. EI and FI are the innermost TGCs, which are used to suppress the fake hits and low momentum background tracks.

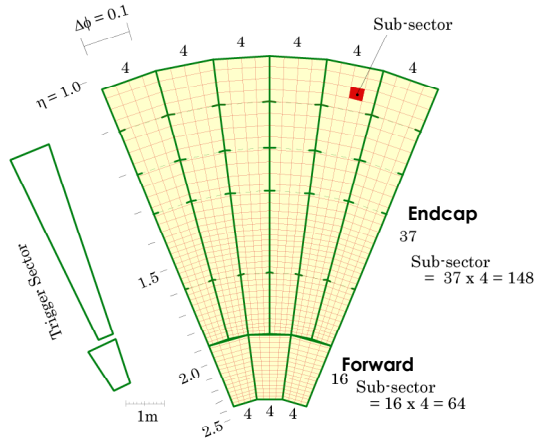

Figure 2: One Eighth of M3 plane (one octant) and trigger sectors.

Figure 2 shows a one eighth of M3 plane (one octant). Each octant is divided radially into 'Forward Region (1.92<η)' and 'Endcap region (1.92>η)'. TGC trigger electronics is divided to correspond to 48 Endcap trigger sectors and 24 Forward trigger sectors on each side.

Due to non-uniform magnetic field, deviations in R and ϕ direction (δR and δϕ) vary among tracks that have same momentum value but through different points. Furthermore, magnetic field is too weak in some areas to extract the charge and pT information. In order to keep the momentum resolution as high as possible, we divided the endcap plane into sub-sectors for each the momentum is calculated independently. Each Endcap sector contains 148 sub-sectors (37R by 4ϕ) and each Forward sector contains 64 sub-sectors (16R by 4ϕ).

C. *Endcap Muon Trigger Electronics Components*

Figure 3 is a block diagram of endcap muon trigger electronics system for one trigger sector. The system consists of three stages. First stage: low-pT coincidences are checked between doublets in two stations (M2 and M3) and then calculates deviation. Second stage: high-pT coincidences are checked to examine if a hit on the triplet corresponds to the result of the low-pT and then calculates deviation. If there is no valid hit in the triplet, the result from the low-pT is sent to the next stage. Low-pT and high-pT coincidences are performed in R-Z plane and ϕ-Z plane independently and muon track candidates with pT of more than 6GeV/c are picked up.

The Sector Logic at the third stage reconstructs muon tracks three dimensionally by combining two sets (R-Z and ϕ-Z) of track information and tags them to have one of six levels of pT. Then, it selects two highest pT tracks in each trigger sector. The resulted trigger information, Region of Interest (RoI; hit sub-sector number), pT value, charge, are sent to the MUCTPI.

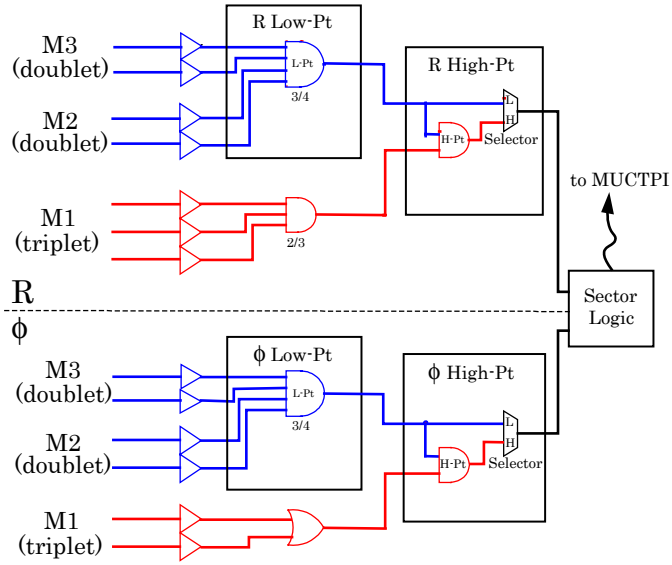

Figure 3: Block diagram of the endcap muon trigger electronics system for one trigger sector.

More details of the Endcap muon trigger system can be found in "First-Level Trigger Technical Design Report [1]" or "First-Level Endcap Muon Trigger System for ATLAS [2]".

II. Design of the Sector Logic

As described above, the Sector Logic has two functionalities: the R-ϕ coincidence and the track selection logic. The R-ϕ coincidence combines the track information from high-pT coincidence; deviation and position, in each sub-sector and identifies each of them to have one of six levels of pT. To calculate charge and pT, we adopted the LUT method because of its flexibility and short latency in calculation. We chose SRAM-embedded type FPGA to hold big LUTs in the same device instead of using external SRAM chips. This design not only reduces chip count and wiring work in the PCB board, but also makes the logic operate faster and results more timing margin.

The track selection logic selects two highest pT tracks in 148 sub-sectors. This selection logic is a kind of priority encoder and the processing speed gets much slower as the number of inputs increases. Therefore, we divided the track selection section into two stages: pre-selectors and a final selector. Each pre-selector collects track candidates along with their pT level assignments from the R-ϕ coincidence and chooses two lowest η tracks. The final selector picks up the final two highest-pT tracks from up to possible 12 tracks from six pre-selectors.

In recent years, FPGA is manufactured with leading-edge technology providing good performance even when compared with that of ASICs. In addition, we can keep an option to easily change algorithm for the track selection logic. There is

no SEU (Single Event Upset) problem of the FPGA device, since the Sector Logic will be located in the electronics hut (USA15; radiation free area).

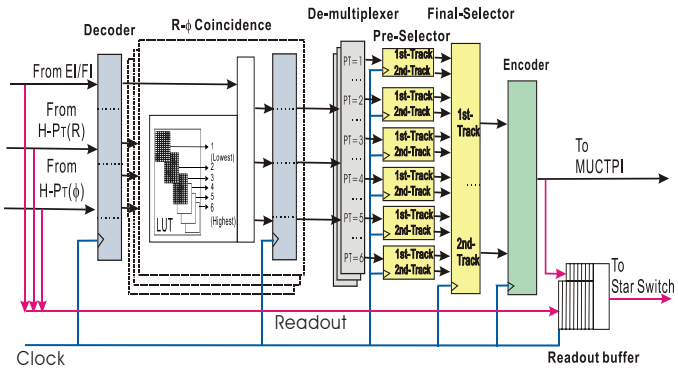

Figure 4: Block diagram of the Sector Logic (for endcap trigger sector). Each block forms a pipeline stage.

Figure 4 is the block diagram of the sector logic (for endcap trigger sector). At the first stage, the decoder block receives serialized data of high-pT coincidences for R and ϕ, which consist of deviations (δR and δϕ) and positions, and are fed to the next stage.

R-ϕ coincidence stage picks up track candidates. If both R and ϕ hits are found in a sub-sector, pT of the track candidate is calculated based on deviations by using LUT method. Then, hits of EI/FI chambers are examined to suppress fake tracks and tracks of low momentum background muons.

Since each high-pT coincidence outputs only one hit among two adjacent sub-sectors, we decided that each LUT covers eight sub-sectors, 2 η rows by 4 ϕ columns, as shown in Figure 5. It is called as Sub-Sector Cluster (SSC). There are 19 SSCs in an endcap sector and 8 SSCs in a forward sector. Each SSC receives one R input and two ϕ inputs at maximum and input data size is 19bits in total. When these three inputs come in an SSC simultaneously, there can be two track candidates. However, there is only one R input for an SSC, either one candidate should be a fake. To solve this problem, we defined that the higher pT candidate is treated as the output of the SSC. An SSC outputs 1bit for charge and 3bits for identified pT levels.

The de-multiplexer distributes track candidates from R-ϕ coincidences are fed to six pre-selectors. Then, each pre-selector chooses two track candidates and the final selector picks up the final two highest-pT tracks among them. Each candidate has position information (RoI number), the charge and the six levels of pT information.

At the encoder block, additional information is added such as bunch-ID number (BCID) and overlap flags. The overlap flag indicates the track pass through the overlap region between Barrel and Endcap chambers to avoid double counting at MUCTPI. The trigger output to the MUCTPI is encoded in the standard 32bit trigger format [3].

The readout buffer sends the outputs from the high-pT Boards and the Sector Logic itself to the Star Switch module (the data concentrator module along the readout path of the endcap muon trigger).

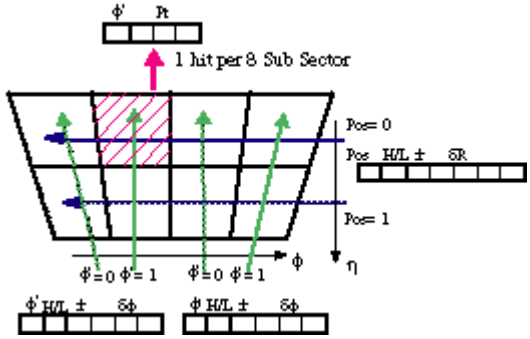

Figure 5: Sub-Sector Cluster (SSC) for the R-ϕ coincidence together with input signal formats. Bit assignment of input and output for the SSC is shown.

III. THE SECTOR LOGIC PROTOTYPE-0 (FOR FORWARD TRIGGER SECTOR)

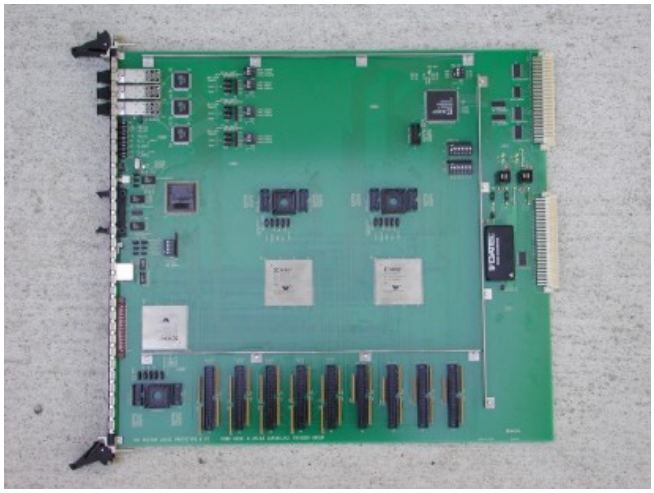

Figure 6: Photograph of the Sector Logic Prototype-0.

We made a fully functional prototype board [4] (shown in Figure 6) to validate the correctness of the Sector Logic design. This Sector Logic Prototype-0 module is designed for forward trigger sector.

Figure 7 shows the block diagram of the Sector Logic Prototype-0. Core logics are implemented in a set of three FPGAs: two FPGAs (XCV405E Xilinx with 560Kbit SRAM) [5] for the decoder and R-ϕ coincidence blocks, one FPGA (XCV400E Xilinx) [5] for the de-multiplexer, 6 track pre-selectors, the final selector and the encoder blocks. Three methods to configure the FPGAs are provided; via VME protocol, via JTAG protocol, and via EEPROM on board.

The input signals (50bits in total) are received via three optical links and de-serialized at the optical interface section. The optical interface section consists of three V23818-K305-L57 (Infineon) OE/EO converter modules and three HDMP-1034 (Agilent) G-Link de-serializers. For readout buffer, a SLB ASIC developed for low-pT coincidence is used.

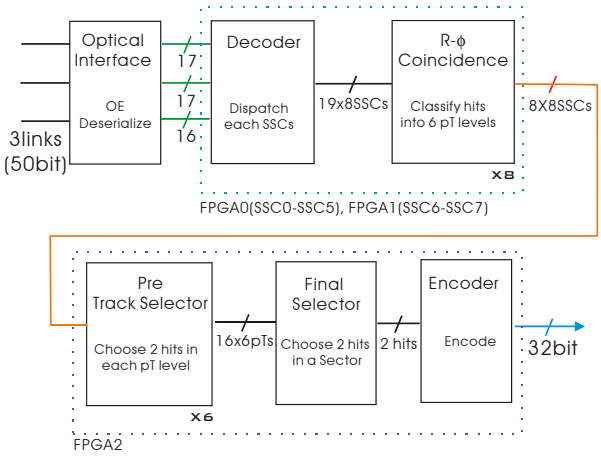

Figure 7: Block diagram of the Sector Logic Prototype-0.

This module is fabricated in a 9U VME 64x module of single width. It is equipped with 160pin(5rows) P1 and P2 connectors, and is a VME64x A32D32 slave module. The power consumption of this module under normal operation mode (@40.08MHz) is ~7W (~2.2A@3.3V).

IV. Tests Results

A. Performance tests

First, we tested the prototype board to validate the correctness of the Sector Logic design. Series of input data were fed to the prototype through an optical interface module with the serializer (G-Link), which was specially made for this test. The output to the MUCTPI was read out. The input and the output were synchronized to 40.08MHz system clock. In this test, a universal clock generator is used. The latency from the G-Link receiver to the trigger output was found to be 7 clocks as expected from the design.

We prepared test vectors, which were simulated the input patterns for the Sector Logic when muon tracks pass the TGCs in region. The test vectors contain up to six muon tracks with various δR and δϕ, and hit position. Therefore, functionality of the track selection logic as well as that of R-ϕ coincidence can be tested. In order to make the test simple, the R-ϕ coincidence was configured with simplified data: if both R and ϕ have a hit, outputs pT value as a function of only δR. 1.3M events were fed and outputs from the prototype were found to be correct without any failure. Therefore, we have justified our design and its implementation for the prototype.

Next, we changed system clock frequency to check that the prototype board run with adequate timing margin at 40.08MHz. We found that it works correctly up to 51.5MHz. At higher frequencies, we found problems on the links between receivers on the prototype and transmitters on the optical serializer module. From this result, we can conclude that the prototype has at least 5.5ns timing margin.

B. Integration test with the MUCTPI

The link between the Sector Logic and the MUCTPI [6] employs 32-bit width LVDS [7]. Timing alignment issues and data integrity through the link were tested to check the trigger data transmission from the Sector Logic to the MUCTPI. This link was found to have adequate reliability at the LHC clock frequency of 40.08MHz. In addition, the interface structure (between the two systems), signal bit assignments, signal levels, was found to conform to that defined in Reference [3].

The FPGA design of the Sector Logic was once configured so that test pattern data words loaded in registers were sent to the MUCTPI. The encoder and driver parts of the FPGA design were un-changed from the original design. There was no bit error occurred during 10^9 events trigger data transmission. Details of these tests are reported in ATL-DA-TR-0004 [8].

V. Conclusions

We made a fully functional Sector Logic prototype for forward trigger sector. The Sector Logic consists of R-ϕ coincidence and track selection logic. We implemented them in a set of three FPGAs. We chose SRAM embedded type FPGA to hold large LUT data for R-ϕ coincidence in the same device. The module was designed in pipelined structure and latency from the G-Link receiver to the trigger output was found to be 7clocks.

We tested the prototype by checking output from the prototype on more than 1M input patterns. The prototype module worked very well with no errors. We found that the system had at least 5.5ns timing margin at 40.08MHz as it worked properly up to 51.5MHz. We also checked data transmission from the Sector Logic to the MUCTPI and found it had high reliability.

From these tests, we conclude that the design of the Sector Logic and the prototype implementation satisfies all requirements for the endcap muon Sector Logic.

VI. Acknowledgements

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VII. References

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