Chamber Service Module (CSM1) for MDT.

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Abstract

CSM-1 is the second and latest version of the high speed electronic unit whose primary task is to multiplex serial data from up to 18 ASD/TDC cards located at the ends of the Monitored Drift Tubes. Each CSM will capture data from all 24 channel TDC (AMT-2 units) of a given chamber and transfer it along a single optic fiber to the MROD, the event builder and readout driver. The core of the board is a Xilinx VirtexII FPGA which will use JTAG protocol (IEEE Std. 1149.1) for logic configuration parameter loading.

I. Role of the CSM in MDT data transmission

The CSM board is being developed and designed at the Physics Department of the University of Michigan in Ann Arbor for the ATLAS project.

CSM belongs to a series of electronic units which have the purpose to acquire and manage timing data in the Muon Drift Tubes (MDT):

(a) *Hedgehog board:* plugged directly at the ends of the Muon Drift Tubes, it converts time data into voltage (analogic);

(b) *TDC/ASD board ("Mezzanine card* "): it converts data into digital and it sends the "interesting" ones away;

(c) *CSM board:* it acquires data from up to 18 different TDC boards and it multiplexes them to the MROD.

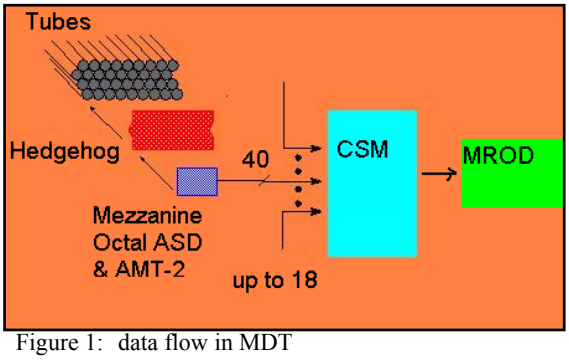

Figure 1: data flow in MDT

Figure 1 shows the path of data from the Tubes to the last unit (MROD).

II. The first Prototype (*CSM0*)

CSM1 is the intermediate step board between the first prototype designed and produced and the final one. The first prototype is mostly known as CSM0 and it has been produced on spring 2000 (a slightly different version has also been designed and produced in 2001 to supply a larger number of institutions and for the H8 Test Beam in Summer 2002). It is composed of two main parts:

⇒ *VME board*: plugged in a VME crate, it communicates with the user through a computer interface and it has RJ45 plugs for the connectors from the 18 TDC's boards;

⇒ *Daughter card*: the core of the unit; plugged into the VME card through two 140 pin connectors, it contains one DPRAM and five FPGA's to manage and output the data acquisition.

In order to have the possibility to analyse the data acquired, thus testing the functionality and accurateness of the ASD/AMT cards (mezzanine cards) as well, the CSM0 prototype not only multiplexes the timing data, but it also groups them in events and saves them in a FIFO.

Moreover the CSM0 emulates the main functions of the TTC unit (Trigger Timing Control) and it programs the mezzanine cards with the required information needed for each different acquisition (such as threshold voltage, time windows).

Figure 2 shows a diagram of the CSM0.

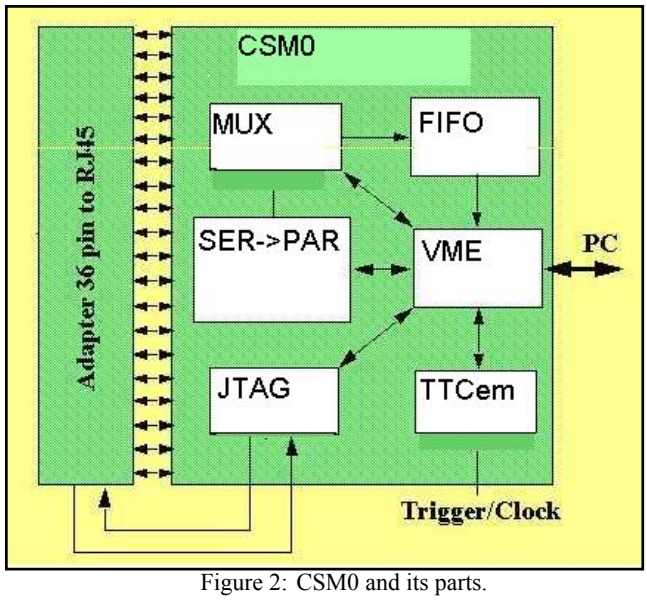

Figure 2: CSM0 and its parts.

III. THE FINAL CSM MODULE

Even though the main task of fast data acquisition and transmission does not change, the global final design is going to have a very different structure, both hardware and software. The software change is mostly an effect of the hardware change, moreover they also both depend on the different units which are going to be used in the final structure.

A fairly detailed scheme of the CSM module can help to understand its parts with its main features (figure 3).

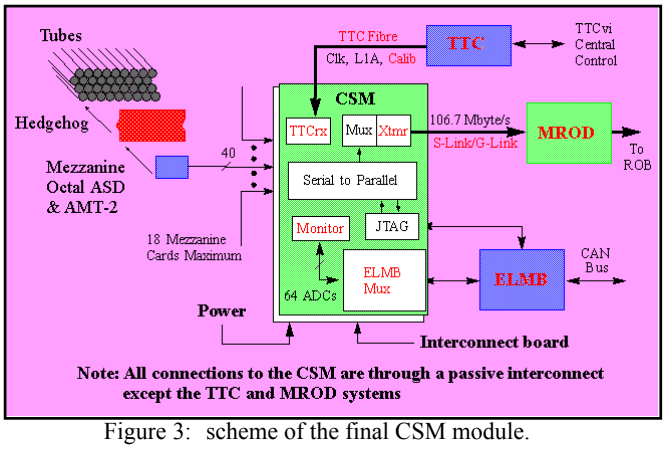

Figure 3: scheme of the final CSM module.

Interconnect board: also called *motherboard*, it provides all the connections to the TDC boards (up to 18) through some 40-pin plugs placed on its bottom side. Besides it has a big power connector installed (up to 16 Amps) which will provide power to the daughter card such as to all the AMT/TDC boards plugged into it. On the top side four 140-pin receptacles are installed where the CSM1 board will be plugged in: they are used to transfer all signals and power to the daughter card.

Two smaller 20-pin connectors will link the unit to the ELMB and they will be used for testing purposes in a first phase. A first small (6 units) stock has been product and is currently being tested before getting ready for the final production (about 1,200 units total at $150 each).

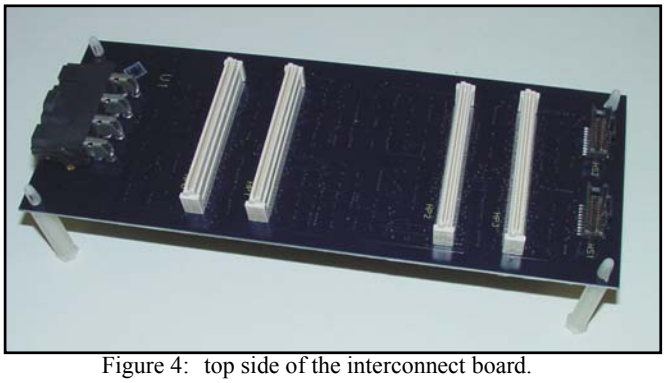

Figure 4: top side of the interconnect board.

CSM board: it is still the core board of the whole unit (like CSM0) but the structure has changed drastically.

CSM1 board is much similar to the final CSM rather than CSM0. The main differences will be shown while describing the board's main units.

Multiplexer:

it is the unit which acquires data from the serial to parallel unit and it sets them ready for the optical transmission. It checks for words availability from each TDC on a rolling procedure and, if present, it sends them away, if not it sends away an empty word. At the end of the 18 data transmission (TDC0 through TDC17) it sends a spacer word with a collection of all the parity bits extracted from the incoming data words (see below).

TDC 0 Data Word
TDC 1 Data Word
.....
TDC 17 data Word
Spacer
TDC 0 Data Word
.....

Serial to parallel unit:

data are received serially from each TDC, each with its 40MHz clock strobe. The single FPGA unit has to deal with up to 18 different data acquisitions simultaneously with strobes at the same frequency but random phases (depending on the cables' lengths as well). An internal device of the Xilinx II FPGA called DCM is used to overcome the issue: it is a hardware unit which outputs the input clock in its 90, 180 and 270 degrees phases. Thanks to these signals each serial stream can be sampled in the best phase available and the parallel word extracted is saved in an internal small FIFO, ready for its transmission to the optical unit.

Transmission unit:

it receives the 32 bit parallel data from the multiplexing unit and it sends them to the MROD through a fiber optic connection. It is composed of two main components: a Gigabit Optical Link chip (GOL) and an Infineon optical transceiver, used only as a transmitter. The GOL, designed and producted at CERN, is a multi-protocol high speed transmitter ASIC (0.25 μm CMOS technology) and it can send up to 1.6Gbits per second.

A 25 MHz high precision oscillator provides the clock to the transmission unit passing through a delay locked loop inside the FPGA in order to be synchronized with the incoming parallel data. The optical fiber connecting the CSM to the MROD can be as long as 550 meters.

JTAG communication:

IEEE Std. 1149.Boundary Scan (better known as JTAG) provides both the configuration bit streams to the programmable units and the communication (both ways) between the CSM1 module and the external units. Its standard protocol allows the connection with all different components which support it and as a matter of fact a large JTAG chain has been created in including both internal and external parts: external user, flash RAM, FPGA, GOL, 18 AMT/TDC boards.

ELMB multiplexer unit:

it manages all the calibration signals and it sends them to the TDC units; it is not installed in the intermediate prototype (CSM1).

IV. CSM1 Prototype: The board and its parts

CSM1 board's dimensions are 80mm x 130mm and it has both surface mount (SMT) and thru-hole components mounted on both sides of it. Figure 5 shows the final layout of the board as it will look like before the placement of its components.

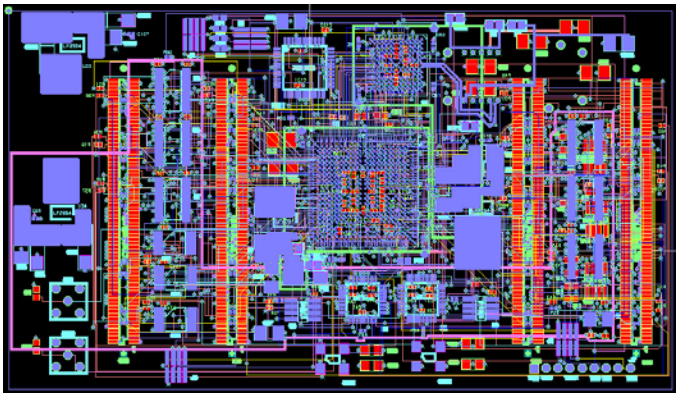

Figure 5: Layout of the CSM1 board.

It is composed of 10 total layers: 7 signal layers and 3 power layers. Since the board needs 3 different power supplies, in order to provide five different power signals (ground, input power from the interconnect board, 1.5V, 2.5V, 3.3V), the least used ones (1.5V and 2.5V) share the same layer with the input power. Traces are 5 miles (0.127mm) wide and clearances between traces and between traces and vias is 5 mils also.

The major challenge of the board is the big number of different signals (about 400) coming from the other external units in such a small space available (the board dimensions are constrained by their final position on the chamber), including a wide range of fields its tasks belong to, from data acquisition and multipexing at the speed of 40Mz per second, to the optical fiber drive. Moreover most of the signals managed are LVDS pairs and they need a particular care in routing them because a not-insignificant difference in the pairs' trace lengths can originate wrong acquisition and/or transmission of data information. To overcome this possible cause of malfunction all the LVDS pairs outgoing from the core unit have been hand-routed in parallel on the same exact route (also by avoiding changes of layers through placement of vias) in two close-by different layers.

Four jumpers will allow to access directly the JTAG chain (thus excluding the optical isolators from the path) such as other four jumpers will allow to "jump" on each of the component originally included in the chain itself. All these options have been included exclusively for a testing purpose.

A. Components of the CSM1 board.

a) Xilinx FPGA.

The field programmable gate array used in the board belongs to the Xilinx *Virtex II* family and its complete part number is *XC2V1000FG456.* This FPGA has 1 Million system gates, it has 456 Input/Output pins with a small size (23mm x 23mm) thanks to the fine pitch ball grid array (FPBGA) geometry (1mm spaced pins set in an array-like structure).

The core has a low 1.5 power supply (with a 3.3V auxiliary voltage as well) and it is divided in 8 fairly autonomous blocks and the I/O pins can be used in many different ways according to the voltage supply of each block; in the CSM1 board only 3.3V LVTTL and LVDS signals are used (see figure 6).

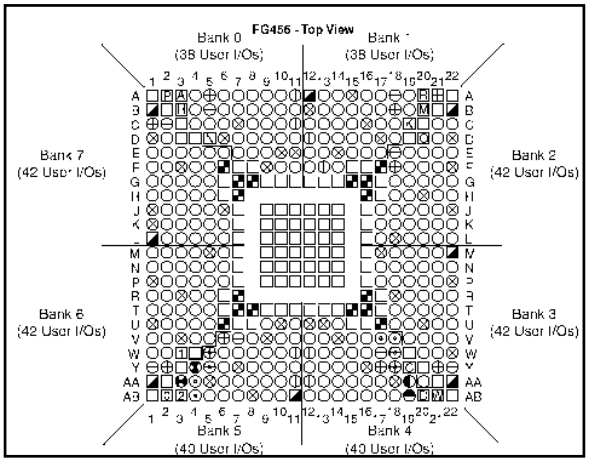

Figure 6: VIRTEX II structure and its 8 blocks.

The DCM (Data Clock Management) units are used to originate the phasing translations of the incoming strobes and as a delay locked loop; the BSCAN_VIRTEX2 is a hardware module internal to the FPGA which, once instantiated in the design, is used for the JTAG transmission of data through two user accessible registers.

b) Xilinx PROM

It belongs to the Xilinx XC18V00 family (exact part number *XC18V04VQ44*) and it is powered with 3.3V supply. It contains the data stream which is going to program the FPGA at power up. The programming of the FPGA can be either in master/serial mode or through the JTAG protocol: the second option is the only available in CSM1. The only way to download the bit code in it is through JTAG. It is not properly a PROM since it is re-programmable up to 20,000 times. The package used is a 44-pin plastic quad flat.

c) Voltage Regulators

Four surface mount voltage regulators are in the board, they all belong to the National LP3964 family (the same used in the AMT/TDC cards) and they can supply up to 800mA each:

- 1.5V: used for the FPGA core;
- 2.5V: for the GOL chip power supply;
- 3.3V: for the FPGA I/O signal (both LVTTL and LVDS) power supply, the FPGA auxiliary power and all the remaining components (optical couplers, fanouts, JTAG parts, transceiver). Two different voltage regulators for this output values are used in order to provide the sufficient amount of power to all the board; they share the same power layer but they are split to avoid bad interference between the two regulators.

Every regulator is connected to a metal plate on the top side of the board in order to avoid their overheating (see the board figure).

d) Optical Isolators.

Four signals are optically isolated for the JTAG transmission: three are inputs to the module (TDI, TCK, TCS) and one is an output (TDO). Three Agilent HCPL063L chips are used (3.3V power supply).

e) Gigabit Optical Link chip (GOL).

It is the interface between the master unit (FPGA) and the physical transmitting component.

It is a multi-protocol high-speed transmitter ASIC. It sustains transmission of data as fast as 1.6GBit/sec and it can transmit data both in Ethernet and G-Link mode, slow and fast transmission (800Mbit/sec vs. 1.6Gbit/sec). Slow transmission is used in the CSM design. It is boundary scan (JTAG) compatible

f) Infineon Transceiver.

It is a small form factor transceiver (Part # V23818-K305-L57); even if it has both reception and transmission option, it is used only as a transmitter. It sends serial data to the MROD according to the SLINK protocol It has a 3.3V power supply and the laser wavelength is 850 nm. The fiber transmission can be as long as 550m.

g) Clock and signal multiplexers and fanouts.

They create copies of the signals coming out from the FPGA and which are repeated for each of the 18 TDCs in order to save some IO pins of the FPGA such as decongestion the crowded routing around the main chip. The multiplexed signals are both LVTTL and LVDS.

V. DESIGN AND PRODUCTION CURRENT STATE.

CSM1 board layout has been completely designed and the artworks (also known as Gerber files) needed for the production of a first stock to be tested are ready to be sent to the board manufacturer. This version of the CSM1 does not have a TTCrx unit installed on it and it is currently under discussion the option to upgrade the version to be produced with the unit. This change will involve a small change in the board design and will allow to get rid of the 40MHz oscillator such as the external trigger and calibration connector.

Upon availability of the TTCrx components and reliable documentation, this modification will take place and only this new version will be sent for production. Therefore the CSM1 will be much more similar to the final version but this will involve a slight delay in the production itself (hopefully two weeks).

The main goal is to have a set of boards of the final CSM, tested and perfectly working, by the summer 2003 Test Beam at CERN.