Level 0 trigger decision unit for the LHCb experiment.

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Abstract

This note describes a proposal for the Level 0 Decision Unit (L0DU) of LHCb. The purpose of this unit is to compute the L0 trigger decision by using information of L0 sub-triggers. For that, the L0 Decision Unit (L0DU) receives information from L0 calorimeter, L0 muon and L0 pile-up sub-triggers, with a fixed latency, at 40 MHz. Then, a physical algorithm is applied to give the trigger decision and a L0Block data is constructed. The L0DU is built to be flexible : downscaling of L0 trigger condition, change in conditions of decision (algorithm, parameters, ...) and monitoring are possible due to the 40 MHz fully synchronous FPGA based design.

I. THE UNIT

The purpose of this unit is to compute the L0 trigger decision of LHCb by using information of L0 sub-triggers (see figure 1).

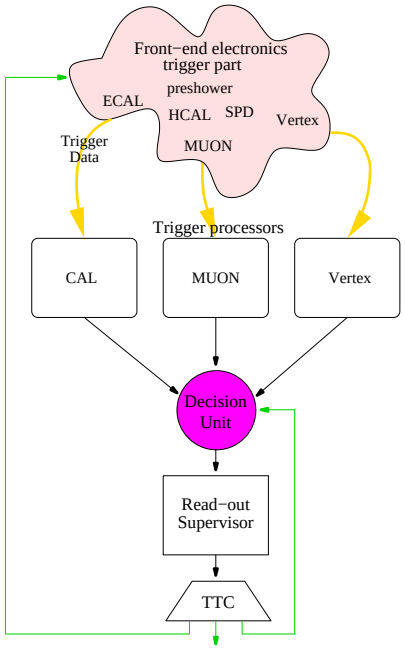

Figure 1: Simplified L0 trigger system

For that, the L0 Decision Unit receives information from L0 calorimeter, L0 muon and L0 pile-up sub-triggers, each with its own fixed latency, at 40 MHz (see figure 1). Then, a physical algorithm is applied to give the trigger decision and a L0block data is constructed. Last, the decision is sent to the Read-out Supervisor system which takes the decision to trig or not. And, under some trigger conditions, the L0block data is sent to L1 trigger and DAQ systems. The TTC system fans-out the decision to the whole experiment.

The L0DU is built to be flexible. Special triggers can be implemented. Downscaling of L0 trigger conditions and change conditions of decision (algorithm, parameters, downscaling, ...) are possible. Monitoring of performances with 42 bit counters will be done and the motive of the decision is coded in an explanation word (L0DUrpt).

The baseline is to exchange data with a serial LVDS protocol.

The mean frequency of the L0 trigger is 1 MHz.

Special care of the good running and debugging of this unit has been taken and a dedicated test bench able to test the good behaviour of the L0DU will be permanently available.

Table 1: L0DU port summary

External system	**I/O**	**# bits**
CAL	I	224@40 MHz
MUON	I	256@40 MHz
VETO	I	64@40 MHz
spare	I	96@40 MHz
RS	O	16@40 MHz
L1	O	1024@1 MHz
DAQ	O	1024@40 kHz
ECS	I/O	N/A

A. Input data

The input data are made up of several “candidates” that correspond to the few highest transverse energy (E_T) or momentum (P_T) detected particles. Thus the calorimeters send one electron, one photon, one local neutral pion, one global neutral pion and the two highest hadrons as candidates. The muon detector sends the two highest muons for each quarter of detector, while the vertex detector transmit the useful data in order to make a veto (no trigger allowed in case of multiple collision) calculation. In addition the total energy deposited in calorimeters is also sent.

The data are sent on 32 bits words including a bunch identification number allowing the synchronization between the data sources since each has its own latency.

A total of 640 bits (see table 1) at a frequency of 40 MHz is expected at input of the L0DU while 16 bits @ 40 MHz are sent at the output.

B. Architecture

For each data source, a "partial data processing" (PDP) system performs a specific part of the algorithm and the synchronisation between the various data sources (figure 2). Then a trigger definition unit combines the information from PDP systems to form a set of trigger conditions based on multi-sources information (see figure 2).

Every trigger conditions are logical ORed to obtain the L0DU decision after have been individually downscaled if necessary.

In parallel, informations from L0 pile-up processor of vertex detector are used for VETO computation and can be used to reject events with more than one interaction per crossing.

Then a decision word (16 bits) is sent to the readout supervisor. This word includes the decision itself (1 bits) and 12 bits for the bunch number. One additional bit is used to ask for a forced trigger for debugging and slow control purpose. Another bit allows timing tuning functions of the Readout Supervisor. It is set when a given pattern of decision is detected over 5 events (the current event and two events before and after). The last bit is reserved for future change.

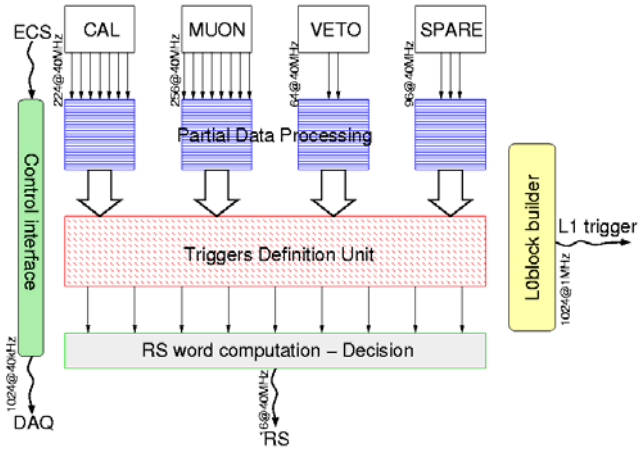

Figure 2: L0DU logical architecture

The L0block builder part constructs and manages L0blocks. The L0block contains up to 32 words of 32 bits of data concerning an event (header, raw input data, processing algorithm partial results, L0Durpt, etc.). It is sent to L1 trigger system only when the experiment L0 trigger is received on the decision unit. For that, the L0block is build for each event then stored into pipe-line memories waiting for the L0 trigger and finally put into a FIFO when validated. Each validated L0block is sent word by word at a 1 MHz frequency (word sent at 40 MHz).

The control interface exploits signals delivered by the ECS to manage the algorithm parameters, the data processing algorithm behaviour, reset scenarios, slow control, on line debugging and monitoring and many other tasks like FPGA programming.

Like a detector front-end electronic board, the decision unit is able to send data to the DAQ system when an event is validated by both L0 and L1 triggers. Thus the decision unit implements some DAQ functions (L0 pipe-line, L1 FIFO and interface to the standard readout system).

C. I/O format

The electrical levels will be LVDS. It is foreseen to use RJ45 connectors with CAT5+ Ethernet cables for every trigger processor. Nevertheless, in order to reduce the number of incoming cables and connectors, the data will be serialized. In this note the baseline is to exchange data with the L0 sub-triggers with a serial LVDS protocol. This limit the link length at a secure value of 20 meters in order to guaranty data integrity.

Serialization by a factor of 5 using DS90CR215 and DS90CR216 chips from National Semiconductor allows cable length to reach 20 meters. Some more accurate tests have to be performed to qualify and validate this solution (several links working together). This solution is envisaged to dramatically reduce the amount of connectors as up to 21 bits could be sent on one RJ45 connector. DS90CR483 and DS90CR484 chips could also be used to transmit 48 bits on 9 twisted pairs. The technology is improved to satisfy signal integrity requirements (pre-emphasis) while the serialized data clock is 240 MHz. In this case, the serialization process takes only 1 clock cycle. The serial LVDS solution is preferable and could be used for each sub-L0-trigger.

In any case, it is tried to use only one electrical standard on the whole L0DU interfaces in order to simplify test and maintenance procedures. If we take into account the input data width of a LVDS serializer and if at least one serializer is used per candidate, the best normalized trigger processor data word width would be either 21 or 48 (or a multiple of these values).

Serial LVDS links have been tested at LAL (IN2P3/CNRS, Orsay, France).

D. Flexibility

For the design, an emphasis is put on flexibility. The use of FPGA makes this point easy to implement. As the data processing algorithm remains quite simple, most of the probably needed functionalities (specific trigger conditions for example) can be implemented and then selected by the way of configuration registers, without the need of a dedicated complex configuration software associated to fully configurable architecture. In case the algorithm has to be greatly modified, the FPGA could be re-programmed.

II. FUNCTIONNALITIES

The L0DU is based on very simple algorithms mainly formed with some cuts on energy or impulsion of the

candidates. Of course the type of selected physical event is conditioned by the applied algorithm. As an example, calorimeter candidates by applying a threshold on E_T can be used to select b events while total E_T can allow to reject multiple interactions. A lot of others simple trigger conditions can be foreseen. A set of conditions gives the behaviour of the unit in term of "trigger-able" events. Many set of conditions can be programmed and swapped on-line.

Some more complex tasks can be implemented : data synchronization, synchronization cross-checking, search for the 3 highest muons over the 8 candidates, sum of the highest P_T muons, invariant mass calculation, combination between simple conditions to produce fine triggers.

The final decision is based on intermediate decisions (realization of a simple or a complex condition). Each intermediate decision can be masked (no more taken into account), downscaled (the corresponding conditions are temporary relaxed) or rate divided (only a given percentage is accepted).

Other functionalities have also to be implemented. They do not concern directly the decision algorithm. The algorithm parameters downloading permit to tune up the L0DU behaviour. A DAQ interface allows to output all the needed data for off-line analysis (mainly the inputs and the outputs of the unit and some intermediate results like the L0DUrpt). The L0Block communicates to the level one trigger system a set of information which allows the L1 decision refinement. The most important is probably the on-line monitoring functions though ECS : 42 bits counters provide some statistics on taken decisions and intermediate results can also be transmitted to a computer for on line functional validation (based on low frequency arbitrary sampled data).

The latency (time between the last input word of an event and the corresponding decision) of the unit is fixed to a maximum of 525 ns including output drivers and cables.

III. L0DU Test Bench

The tests of L0DU and the test bench are more complex than the unit itself. Test structures had to be ready before the design completeness of the unit and, all the more reason, of the first prototype of the unit.

A. Test bench prototype

Thus a L0DU test bench prototype was designed. It is made up of several "memory" boards synchronized by a "clock generator" board. Each board allows 64 bi-directional input/outputs to be driven or received into standard CAT5+ Ethernet cable and RJ45 connectors with LVDS levels at a 40 MHz frequency. The memory boards are both used to store the stimuli and the outputs of the tested system. The maximum number of data words is 2^{16} for the moment.

The user defined stimuli and the data from the system under tests are downloaded or read out through a VME bus by a dedicated computer (software written in C and LabView) at a low speed.

The user can configure the number of words to transfer, start and end address, the number of stimulation cycles. The latency introduced by the system under test is compensated.

In addition, the clock generator board delivers a synchronization signal as a reference for the whole test bench timing. Up to 16 memory boards can then be put in time. The clock generator outputs format are LVDS or ECL. It produce various other clock signals : half and quarter frequency signals , low frequency signal for trigger generation. The master clock is either 40 or 60 MHz.

B. Memory board design

The main component is a FPGA ACEX1K100 (Altera). It implements a VME interface (A24/A32, D16/D32 compatible), manages the four 16 data bits SRAM (address, control signals) and configures the data path according to the current task of the memory board (see figure 3).

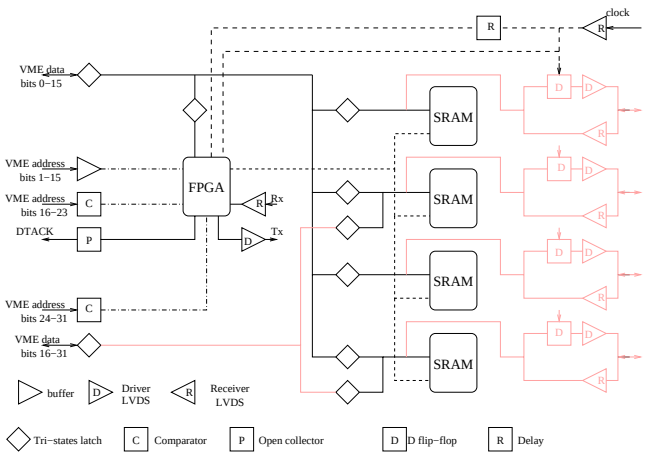

Figure 3: memory board architecture

When the stimulation is running, the board is autonomous and does not need to be controlled through the VME system if it is correctly configured however.

In order to allow new stimulation cycles with a minimized dead time, initial conditions of the run are restored immediately after that the previous cycle ends.

The interfaces on the tested system side are bi-directional in order to minimize the amount of connectors. In the case of data emission the cables are then adapted at both ends (the parallel adaptation resistor is already present at the interface). It limits the cable length to a value of about 20 m for both data emission and reception.

C. Future versions

Three copies of the memory board are being used to perform the test of the first prototype of L0DU. They are working properly but a few improvements are planned : the increase of the number of stimuli that can be stored or acquired and the use of a serial LVDS format to be compatible with the final version baseline (bi-directional

ports not allowed). With external electrical format adaptation modules, the memory board could be adapted to many interface types.

D. Embedded test bench

A simplified version of this external test bench is foreseen to be integrated on the L0DU. It will allow to ensure that the L0DU is still working correctly by injecting some data patterns determined to make an easy diagnostic of the possible problems. Such *in situ* tests will be realized as frequently as possible when the normal physics data acquisition is stopped (for example between two runs). Meanwhile the full debugging and the maintenance will be performed with the external test bench. In that way, a few copy of the L0DU will be permanently maintained to ensure the full availability of the unit.

A migration to the ECS standard systems and software will be envisaged for the embedded test bench.

As for the memory boards, the embedded test structures will be based on external RAM chips.

IV. L0DU First Prototype

A first prototype was designed at the beginning of year 2002. The first L0DU prototype is a simplified version of what is foreseen to be the final L0DU at this time.

The first prototype is aimed to test algorithm, functionalities, data flow and should help us to evaluate the L0DU needs about ECS. In order to perform a quick design, the first prototype is fitted into FPGAs and has a reduced number of inputs (96 bits) and outputs (32 bits) in LVDS format (40 MHz) allowing a direct connection with three memory boards for test purpose. Cables and connectors will be respectively CAT5+ and RJ45. This prototype will offer a maximum flexibility and adaptability to test a large part of the final L0DU functionalities including L0block building operations.

A. Design

The critical point for L0DU and for its prototype is the number of interconnections between on one hand the external systems and the L0DU and on the other hand the various elements that form the unit. It is not expected that the final version would be constituted by more than one board in order to limit interconnection failure between constituents.

For the prototype, the use of a single up-market FPGA is sufficient in term of number of input/output and internal memory resources. Nevertheless to avoid the use of BGA package (ease of test) and to be more realistic in relation to the final version, the prototype is made up of five interconnected ACEX1K100. Each FPGA includes about 50 kbits of RAM, provides up to 147 user input/output and allows 100k equivalent gates design to be fitted in.

The prototype does not have any ECS or TTC system. It acts like a 40 MHz pipelined flow through system.

The L0Block building structures use a large part of the available internal memory. As the experiment level L0 trigger decision is distributed a rather long time after the raw data are produced, a few DAQ-like channels have been implemented. They are made up of a pipeline memory to make the data waiting the L0 trigger, followed by a FIFO memory used to store the validated L0Block data to be send to L1 trigger system. No external memory is needed. This point allows a more simple PCB and the i/o ports usage optimisation (low number of additional control signals).

B. Algorithm example

In the following, one of the simple algorithm implemented and tested in the prototype is described.

Four candidates are sent to the prototype (1 electron, 2 hadrons and 1 muon). In addition the global ECAL energy and a VETO word (from vertex detector) are transmitted. The various sources latencies are simulated.

After a first synchronization step, few thresholds are applied on the data (electron, muon and first hadron). Each threshold constitutes a simple intermediate condition for a positive trigger. An additional “complex” intermediate condition requires that the two hadrons momentum reach a corresponding threshold at the same time.

Each intermediate condition is individually downscaled, rate divided or masked under a given set of parameters (8 sets are programmed).

Finally the decision is taken if the three following final conditions are realized : no veto from the vertex detector, global ECAL energy below a maximum threshold and one or more intermediate condition validated.

In parallel, the L0Block is built and stored in 24 DAQ-like storage structures, the decision word is sent to the readout supervisor and the L0DUrpt is built (sent to DAQ, ECS and L0Block).

Other algorithms were implemented and successfully tested. Due to the synchronous pipe-lined architecture they should be easily scaled to the final version of the unit. Recent up-market FPGA technologies providing more input/output ports in many formats and more internal memory will be used.

V. Conclusion

The figure 4 shows the first prototype of the decision unit being tested with 3 memory boards and one clock generator. The test bench is controlled by a PC running under LINUX with a C++ software and a PCI/VME interface.

The test procedure has shown that the whole system works perfectly. The L0DU design can be carried on by adding DAQ, TTC and ECS systems.

Figure 4: prototype test set-up

VI. REFERENCES

[1]R. CORNAT et al. “Level 0 Decision Unit for LHCb”, LHCb note 2001-xxx, TRIG

[2]R. JACOBSSON et al. “Readout Supervisor Design Specifications”, LHCb note 2001-012, DAQ

[3]J. CHRITIANSEN “Requirements to the L0 Front-end Electronics”, LHCb note 2001-014

[4]C. BEIGBEDER "The front-end Electronics for the Calorimeter Triggers", LHCb note 2000-010

[5]M. BARGIOTTI "The Selection Crate for the Calorimeters trigger", LHCb note 2000-018

[6]E. ASLANIDES "A synchronous Architecture for the Muon Trigger", LHCb note 2001-010

[7]E. ASLANIDES "Specifications of the Muon Trigger Processing Board", LHCb note 2002-003

[8]LHCb talks