Readout Control Unit of the Front End Electronics for the ALICE Time Projection Chamber

R. Esteve Bosch[1], R. Campagnolo[1], H. Helstrup[3], A. Jiménez de Parga [1], J. A. Lien[1,2,3], B. Mota[1], L. Musa[1], D. Röhrich[2], B. Skaali[4], K. Ullaland[2], A. S. Vestbø[2], D. Wormald[4] for the ALICE Collaboration

[1] CERN, Geneva, Switzerland, [2] University of Bergen, Bergen, Norway, [3] Høgskolen i Bergen, Bergen, Norway, [4] University of Oslo, Oslo, Norway

Abstract

The readout electronics for the ALICE TPC detector consists of 4356 front-end cards (FECs) that contain the complete chain to readout the signals coming from 570132 pads. The front-end cards are grouped in 216 readout partitions, each controlled by a Readout Control Unit (RCU) that interfaces the FECs to the DAQ, the Trigger, and the Detector Control System. The RCU broadcast the trigger information to the FECs, collects the trigger related data from the FECs, assembles a sub-event, compresses the data and sends the compressed packed sub-event to the DAQ via the ALICE Detector Data Link (DDL). The RCU is designed to cope with a maximum data throughput of 200 Mbyte/s. In this paper we present an overview of the requirements, the architecture and some of the main design features of the RCU, as well as a description of two RCU prototypes.

I. INTRODUCTION

The ALICE Time Projection Chamber [1] (TPC) is a large gas cylinder (88 m^3) divided in two drift regions by a central electrode located at its axial centre. A field cage creates a uniform electric field along each half of the chamber. Charged particles traversing the TPC volume ionise the gas along their path, liberating electrons that drift towards the detector end plates where multi-wire proportional chambers, with cathode pad readout, provide the necessary signal amplification. Each of the two readout planes is azimuthally segmented in 18 trapezoidal sectors.

The front-end electronics [2] for the ALICE TPC consists of 570132 channels. A single readout channel is comprised of three basic functional units: 1) a charge sensitive shaping amplifier, which transforms the charge induced in the pad into a differential semi-gaussian signal; 2) a 10-bit 10-MSPS A/D converter; 3) a digital circuit that contains a shortening filter for the cancellation of the signal tail, the baseline subtraction and zero suppression circuits, and a multi-event memory. The analogue functions are implemented by a custom integrated circuit (PASA) that incorporates in a single chip 16 channels. The ADC and the digital circuits (for 16 channels) are contained in a single chip named ALTRO (**AL**ICE **T**PC **R**ead **O**ut) [3]. The maximum number of samples that can be continuously processed for each trigger (event data stream) is 1000. Upon arrival of a first level trigger, the data stream is stored in the multi-event memory. This memory has the capacity to store either 4 events, if the event data stream is longer than 512 words, or 8 events otherwise. When the second level trigger (accept or reject) is received, the latest event data stream is either frozen in the data memory until its complete readout takes place, or it is discarded. The complete chain is contained in the Front-End Card (FEC) [4], each containing 128 channels, which are located some 10cm away from the pad plane and are connected to it by capton cables. In total the TPC is equipped with 4356 FECs grouped in 216 readout partitions, with 6 partitions per TPC sector, each controlled by a Readout Control Unit (RCU).

As shown in figure 1, the RCU interfaces the FECs to the Data Acquisition System (DAQ), the Timing and Trigger System (TTC) and the Detector Control System (DCS). The RCU broadcasts the trigger information to the FECs, collects the trigger-related data from the FECs, assembles a sub-event, compresses the data and sends the compressed packed sub-event to the DAQ via optical fibre, the ALICE Detector Data Link (DDL) [5]. Moreover, the RCU has to initialise the FECs and monitor their behaviour reporting to the DCS any detected fault.

The radiation load on the TPC is low, with a total dose received over 10 years of less than 1Krad and a neutron fluency of less than 10^{11} n/cm^2. Thus standard radiation-soft technologies are suitable for the implementation of this electronics. However, some special care should be taken to protect the system against potential damages caused by Single Event Effects (SEEs).

II. RCU ARCHITECTURE

The RCU has the following functional requirements:

I. Distribution of the trigger and clock signals to the FECs.

II. Initialisation of the FECs, including pedestal values, digital filter coefficients, zero suppression threshold, etc.

III. Readout of trigger related data from the FECs, assembly of a sub-event, compression of the data and transfer to the DAQ via the ALICE Detector Data Link (DDL).

IV. Supervision and monitoring the data flow and the status of the FECs: power state, temperature, exception and error conditions, etc.

In this section we discuss each of the above functions and the corresponding interfaces.

A custom bus, the ALTRO bus [6], implements the main communication between the RCU and the FECs. The ALTRO bus is essentially an extension of the FEC's internal bus that allows the RCU to access the FEC's internal components. It is a multi-drop single-master bus where the RCU is the master unit and the FECs are the slaves. In order to minimize the length of the bus cables the RCU supports two branches running in opposite directions. From the electrical point of view the ALTRO bus is based on the GTL/GTL+ technology. All the RCU functions (I-IV) can be performed by means of the ALTRO bus. The ALTRO bus features a bandwidth of up to 200 Mbyte/sec. As shown in figure 1, an independent Control Network [7] establishes a dedicated bus connection between the RCU and the FEC, in view of monitoring and controlling (function IV) the FECs without interfering with the readout procedure. This Control Network is based on the I2C protocol, enhanced with an extra line for handling interrupts from the FECs, and supports a bandwidth of 3.4Mbit/sec.

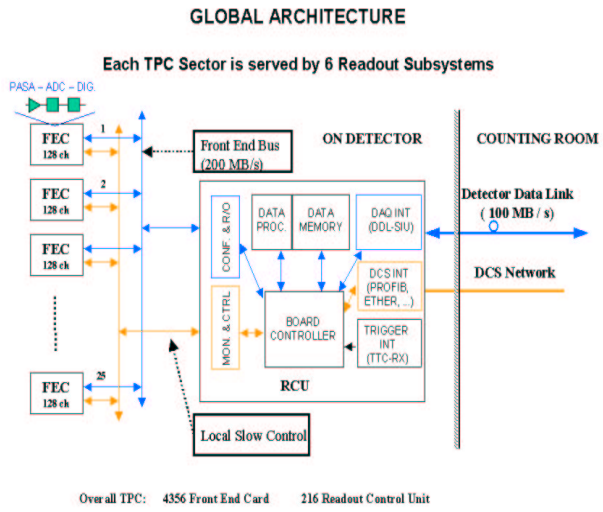

Figure 1: Block diagram of the TPC readout partition. The RCU interfaces a group of up to 25 FECs to the DAQ, the DCS and the TTC. The overall TPC readout consists of 216 readout partitions.

The interfacing of the RCU to the Trigger and the DAQ follows the standard data-acquisition architecture of the ALICE experiment [8]. The ALICE standard to transmit data off detector is the DDL technology (optical fibre). It implements a full duplex interface between the RCU and the Read Out Receiver Card (RORC), which is the first stage of the DAQ and is located in the experiment counting room. The DDL provides the RCU with a bandwidth of 100Mbyte/sec in the RCU→RORC direction and 10Mbyte/sec in the RORC→RCU direction. The DDL is composed of three hardware items: the Source Interface Unit (SIU), which is incorporated in the RCU, the fibre, and the Destination Interface Unit (DIU), which is part of the RORC. The SIU is a CMC-format mezzanine card plugged on the RCU as a daughter board.

The RD12 TTC [9] system is the ALICE standard used to distribute trigger and clock information. Every RCU implements an appropriate receiver (TTCrx), which produces the phase-corrected LHC clock, Level-1 trigger and Level-2 accept/reject. These are used on the RCU, and also distributed to all the FECs via the ALTRO bus. In addition, the TTCrx delivers event identification information to be added to the sub-event header before sending the data to the DDL.

For the communication between the RCU and the DCS two technologies are under investigation: Profibus and Ethernet.

III. RCU CONTROL LOGIC

The control logic of the RCU is divided into multiple state machines (see figure 2). The Resource and Priority Manager is the master state machine, controlling all subsystems.

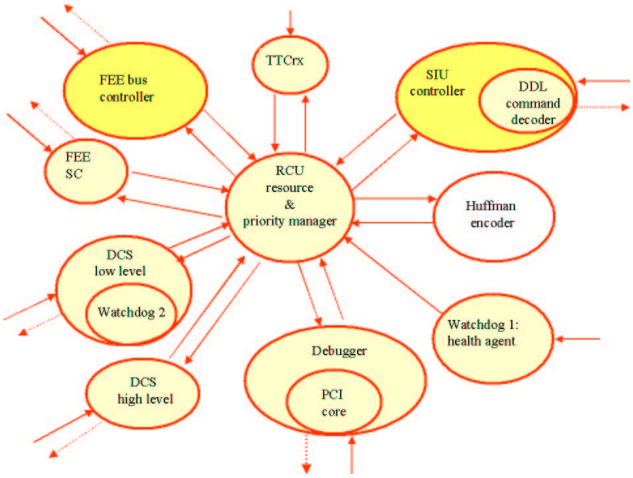

Figure 2: Flowchart of the RCU control logic. The Resource and Priority Manager is the master state machine, controlling all subsystems.

A. *ALTRO Controller*

Uses a custom protocol to service two ALTRO bus branches and all ALTRO chips. It builds and verifies ALTRO commands. The readout sequence of a TPC event is built up from information, stored in look-up tables, about the enabled and disabled channels. The amount of data received is counted and cross-checked with the block length transferred by each individual ALTRO chip.

B. SIU Controller.

It transfers blocks of data form the RCU memory into the DDL SIU by means of the DDL protocol. Each block of data contains one TPC sub-event. It also receives data from the DDL to be stored in the RCU memories or control registers.

C. *Trigger Manager (TTCrx).*

Manages the reception and distribution of triggers from the TTCrx chip. During the dead time of the TPC read out, incoming triggers are blocked. The TTCrx also supplies information that will be included in the Data Header of each sub-event. The Data Format of this header is an ALICE standard described in [10]. The Trigger Manager includes also

the logic to compare the number of triggers received by the RCU and by the ALTRO chips.

D. RCU Resource & Priority Manager.

The *Resource & Priority Manager* defines the priority of the incoming commands to the RCU. The standard operating mode of the RCU is the readout of TPC data from the ALTRO chips. The readout of one event is initiated by the reception of a Level-2 trigger from the TTCrx. The readout is controlled by the RCU. However, the data transfer from the ALTRO to RCU cannot be split in pieces. Thus the memory manager of the RCU must ensure that sufficient memory is available before starting a new data transfer. Whenever needed, the operator can ask to reconfigure either the RCU or the ALTRO chips. A request is sent to the *Resource & Priority Manager* that executes the configuration only after finishing the ongoing readout. Incoming requests are executed, under the control of this state machine, during dead time in readout.

E. *FEE Slow Control.*

Operates a dedicated bus connection between the RCU and the Board Controller in each Front End Card (FEC). This is used for voltage and temperature probing, protocol and multi-event buffer errors reporting, and statistical data read out.

F. Detector Slow Control.

It accesses in write/read mode a set of RCU registers dedicated to store the values of the control/status parameters of the overall system (power state, temperature, error messages, etc.). It connects the FEC's Control to the DCS system.

G. Huffman decoder (optional).

Compression of data can be done on the RCU to make effective use of the available bandwidth and/or memory. An algorithm for Huffman coding has been developed and tested [11, 12, 13].

H. *Watchdogs.*

Health agents, internal and external, that verify and monitor the functionality of the RCU FPGA. SRAM based FPGAs are vulnerable to radiation SEU. If the watchdog reports malfunction, reconfiguration of the FPGA can be done by either onboard or external configuration options.

I. *Debugging interface.*

PCI core for development and debugging. Optional in the final version.

The development of the RCU Control Logics is done using Mentor Tools (FPGA Advantage, ModelSim, Leonardo) and ALTERA Quartus II. Behavioural models (VHDL or Verilog) are used as test benches for the development of the interface state machines.

IV. RCU PROTOTYPE

In this section we describe two RCU prototypes that have been developed and tested with the rest of the TPC electronics components.

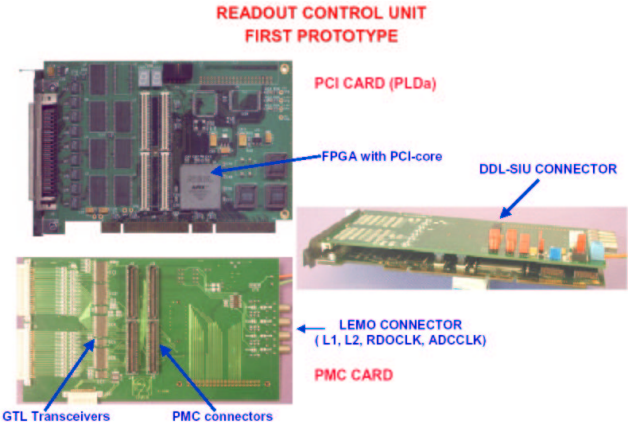

Figure 3: RCU Prototype I. This prototype is based on a comercially available PCI cards (PLDApplications) and a custom-made mezzanine card, which implements the interface to the FECs and the DDL SIU.

A first prototype of the RCU (pRCU-I) has been developed using the ALTERA EP20K400 FPGA on a commercial PCI-board (PLDA) [14]. The ALTRO protocol, a memory controller (FIFO structure) for accessing internal and external banks, and the SIU interface have been implemented in the FPGA and successfully tested. The set-up for the test of the complete readout chain is shown in figure 4.

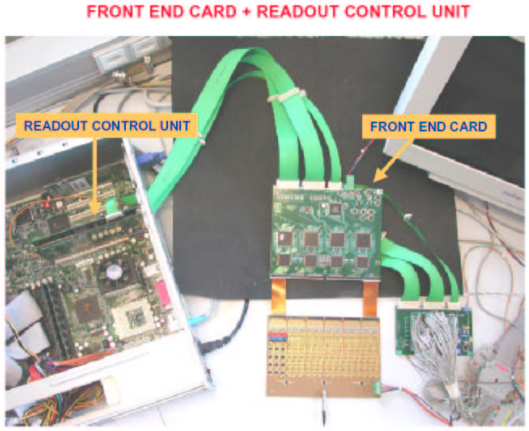

Figure 4: Set-up for the test of the ALTRO electronics. The RCU-I prototype is plugged in a PCI-slot of the PC on the left. One FEC is connected to the RCU via the ALTRO bus prototype.

A second prototype of the RCU has been developed and is being tested. The prototype is based on a PCI motherboard carrying two mezzanine cards, an SIU board and a board interfacing the two FEC-busses, the TTCrx and the DCS system. In this board all components required in the final design are connected to the FPGA. The FPGA I/O-pins are

connected to 7 PMC connectors on which are plugged the two mezzanine cards.

The external memory configuration is optimised to meet the RCU requirements. Indeed, the memory is organised in 2 banks with separate data and address lines. This architecture allows the sub-event building of one event while transferring to the DAQ the previous event. The processing of the event includes adding a data header (including event length, identification and status) using the ALICE standard data format. Meanwhile, the sub-event stored in the other memory bank can be Huffmann-encoded (compressed) and pushed into the DDL. Another use of this prototype is to test different hardware options for the Detector Control System (DCS).

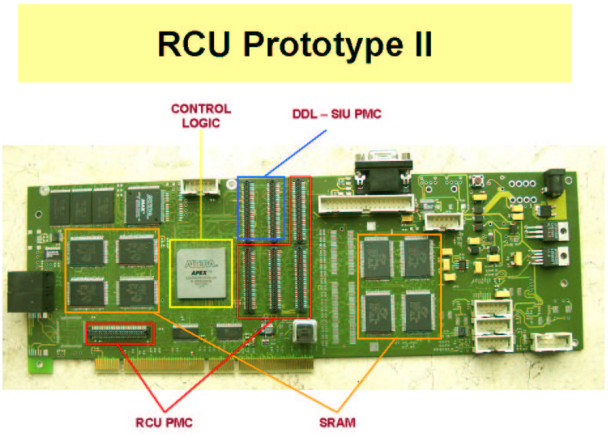

Figure 5: RCU Prototype II layout. SRAM is organised in 2 banks with separate data and address lines. The control logic is contained in the onboard FPGA. The 7 PMC connectors are used to connect to the FPGA two mezzanine boards: the DDL SIU card and the FEC interface mezzanine card.

V. CONCLUSIONS

The RCU plays an important role in the readout and control of the ALICE TPC front-end electronics. It interfaces the front-end cards, which contain the complete readout chain to amplify, digitise process and buffer the detector signals, to the DAQ, the Trigger and DCS. Besides the initialisation and readout functionality the RCU provides features to diagnostic errors and hardware faults.

A first prototype of the RCU has been developed by using a commercial PCI-board (PLDA), based on an EP20K400 FPGA, and a custom PMC board. This first prototype (pRCU-I), which incorporates only the interface to the FECs and to the DAQ, has been successfully used to validate the FEC and ALTRO bus design. A second prototype (pRCU-II), based on a PCI motherboard carrying two mezzanine cards, incorporates all the RCU functions and will be tested with a significant amount of the TPC electronics in the near future.

VI. REFERENCES

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