Aluminium Microcable Technology for the Alice Silicon Strip Detector: A Status Report

V. Borshchov, A. Boiko, S. Kiprich, L. Kaurova, S. Listratenko, G. Protsay, A. Reznik, V. Starkov
SRTIIM, Kharkov

A.P. de Haas, A. van den Brink, P. Kuijer, G.J.L. Nooren, C.J. Oskamp
NIKHEF, Utrecht/Amsterdam

D. Bonnet, J.P. Coffin, C. Gojak, M. Guedon, J.R. Lutz
IReS-IN2P3/CNRS-ULP

M. Bregant, L. Bosisio, P. Camerini, G.V. Margagliotti
Universita di Trieste/I.N.F.N. Trieste

N. Grion
I.N.F.N. Trieste

M.J. Oinonen, Z. Radivojevic
Helsinki Institute of Physics

For the ALICE collaboration

ABSTRACT

All interconnections in the ALICE Inner Tracker Silicon Strip Layers are realised using kapton/aluminium microcables, Tape Automated Bonding (TAB) and soldering techniques.
The major advantages are the reduction in material budget and the increased mechanical flexibility as compared to traditional wirebonding.
Since the last reports (Snowmass LHC workshop '99) considerable progress has been made and designs have been refined and adapted to facilitate production, which will start early next year.
This paper describes the design of the three major interconnection parts:

- The TAB-frame chipcable connects the front-end chips to the detector and to the flex. These cables are mounted in carrier frames for testing and have unique coding to identify cable type as well as coding to check correct alignment in the test connector.
- The flex is essentially a multi-layer interconnecting bus supplying power and control to the front-end chips, with integrated LVDS terminating resistors. The flex is the constructive basis of the hybrid, SMD components can be mounted by soldering or gluing as well as by means of TAB bonds. Ultrasonic bonding and pulsed-bar reflow soldering techniques are used to interconnect the flex to the other parts.
- The laddercable is a 60 cm long cable connecting the front-end modules to the endcaps. This flatcable is designed as a differential stripline for analog and LVDS signals using ultra-low density polyimide foam as spacer material.

Optical and electrical testing of microcables and scanning techniques to inspect TAB-bonds connections are also discussed.

I. INTRODUCTION

The ALICE Inner Tracker (ITS) Silicon Strip Detector (SSD) consists of two concentric barrel-shaped layers (layers five and six) with radius 384 mm and 434 mm respectively. [1]
Each layer consists of approximately one meter long carbon fibre ladders which overlap in RΦ. In total there are 72 ladders, layer five has 34 ladders and layer six has 38 ladders.
Layer five has 22 modules per ladder, layer six has 25 modules. Modules overlap in the Z-direction , each module consists of a double-sided silicon detector with 2x768 strips and two hybrids for the read-out of the P- and N-side.
Six 128-channel HAL25 front-end chips are mounted on each hybrid [2]. This chip is the successor in radiation-tolerant 0.25 µm technology of the ALICE128C chip.
In total there are 1698 modules containing 20.376 front-end chips with 2.6 million channels.
Phynox water-filled tubes (2 mm diameter, wall thickness 40 µm) are used to cool the carbon-fibre hybrids.
Detectors are mounted on the carbon-fibre ladder structure and since the hybrids need to be connected to the cooling tubes, there will be relative movement between these two due to temperature variations.

For heavy-ion physics with very high multiplicities a low-mass design is essential. Furthermore the necessity of overlapping and of water-cooling made the design very complex.
These three points have led to the decision to employ aluminium microcables extensively in the ALICE SSD. These microcables are originally a development of the SRTIIM institute in Kharkov. In the past years this technique has been further refined for the very fine pitches and other requirements needed for use in the ALICE environment.
More information on microcables can be found in two papers presented at the fifth Workshop on LHC Electronics[3],[4] and a poster presentation at the fourth Workshop[5].

II. TAB-FRAME CHIPCABLE DESIGN

To connect the front-end chips to the detector on the input side and to the hybrid flex on the output side chipcables are used. These cables consist of a 10 µm polyimide foil with 14 µm thick aluminium traces. The input side pitch is 80 µm, the output side has 125 µm pitch.
The HAL25 chip layout is optimised for chipcables. On the input side the bondpads do not have the usual staggered row configuration with 40-50 µm pitch, but all input pads are in one row with 80 µm pitch.
The length of the input traces connecting the chip to the detector is 11 mm, the detector pitch is 95 µm so this part also includes a fan-out from 80 to 95 µm.
This input side is the most critical part of the microcable lay-out, the traces are quite long and trace width is just 35 µm. Figure 1 shows a diagram of pull strength versus trace width measured at the SRTIIM lab. Curve 1 is the pull strength attainable if bonding parameters are continuously adjusted for increasing trace width. Curve 2 shows pull strength variations when trace width is varied, but bonding parameters are kept constant at the optimal settings for a 35 µm trace width. There is a reasonable window in which reliable bonds can be made with constant settings, which is important for production on automatic bonding machines.

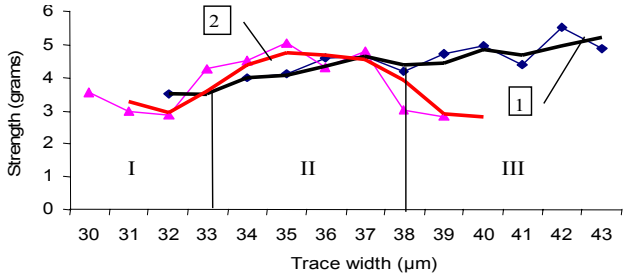

Figure 1: Bond strength graph.

Besides being involved in the setting up of production facilities, the Helsinki group is doing research on the aluminium TAB process, using Laser Scanning Microscope (LSM) techniques and White Light Interferometry (WLI). Goal is to gain better insight in this process and thus increase reliability. Figure 3 shows the measured cross-section of the aluminium trace along the black line of figure 2. An WLI image and a LSM picture of input trace bonds on a chip is shown in figure 2 and figure 4.

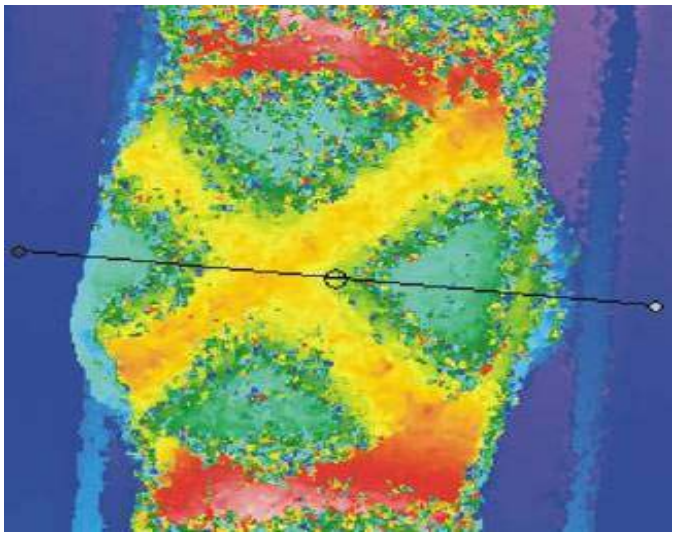

Figure 2: WLI image of TAB bond.

Figure 3: Cross-section of figure 2.

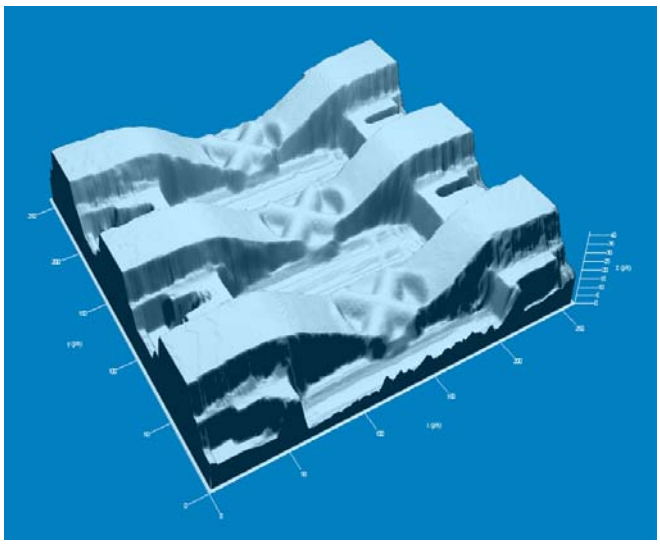

Figure 4: LSM image of TAB bonds.

To increase the bonded chip yield for high volume production, an optical scanning system for chip cables has been installed in Trieste (figure 5).
This is an intelligent scanner, which uses good cables as learning objects and is then able to scan for shorts and breaks in traces with resolution of a few µm. The left picture of figure 5 shows the scanning table which has been designed to scan 24 TAB frames in one run. The right picture of figure 5 shows a scanning detail. De dotted lines mark the boundaries used by the scanning software.

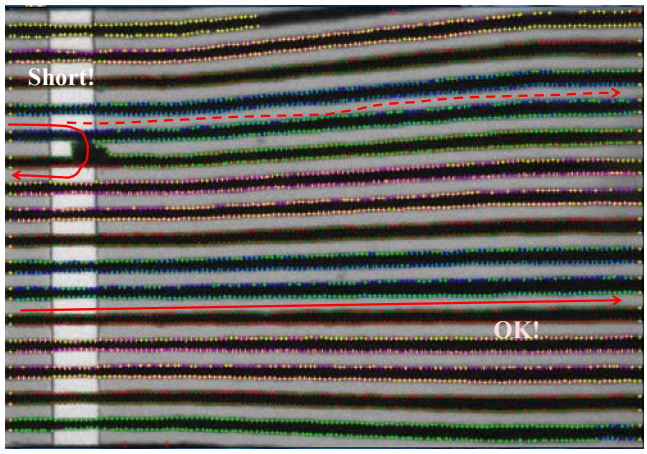

Figure 5: Optical scanning system (left) and chipcable detail (right).

On the output side of the chip, the chipcable is used to connect power, control and read-out signals to the chip. The pitch varies from 125 µm on the chip side to 250 µm on the flex side and the length is 2.4 mm.

To facilitate handling and testing, the chipcables are mounted in TAB-frames. These frames, as well as the testconnectors for these frames, are available commercially. Figure 6 shows the layout of the chipcable. One can see that all the traces coming from the chip are continued beyond the bonding areas to testpads located all around the circumference of the cable

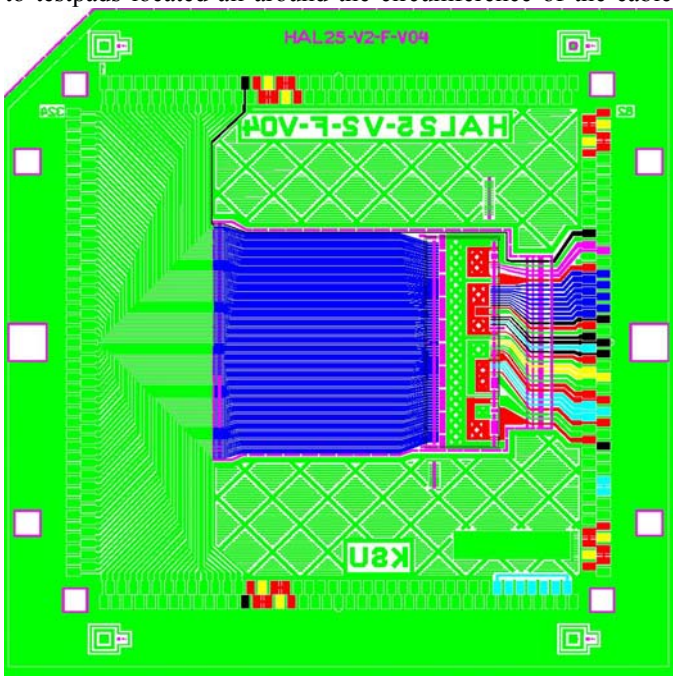

Figure 6: Chipcable design.

template. Only the inner part, confined inside the red* striped line, is retained for final use. The outer part, containing the 324 testpads, is removed before bonding the cable to the detector and flex. Via the testpads and the testconnector all inputs and outputs of the chip are accessible.

The great advantage of this system is that chip, chipcable and bond connections are all tested in one go. The result is a known-good sub-assembly.

In figure 7, a framed chipcable with bonded HAL25 chip is shown. The cable can move slightly in the TAB frame, which has four pins that fit in oversize holes in the cable template. For accurate positioning both the testconnector and the jigs used for bonding and testing, have four metal pins located at the corners of the testpad rows that fit in precise holes in the cable.

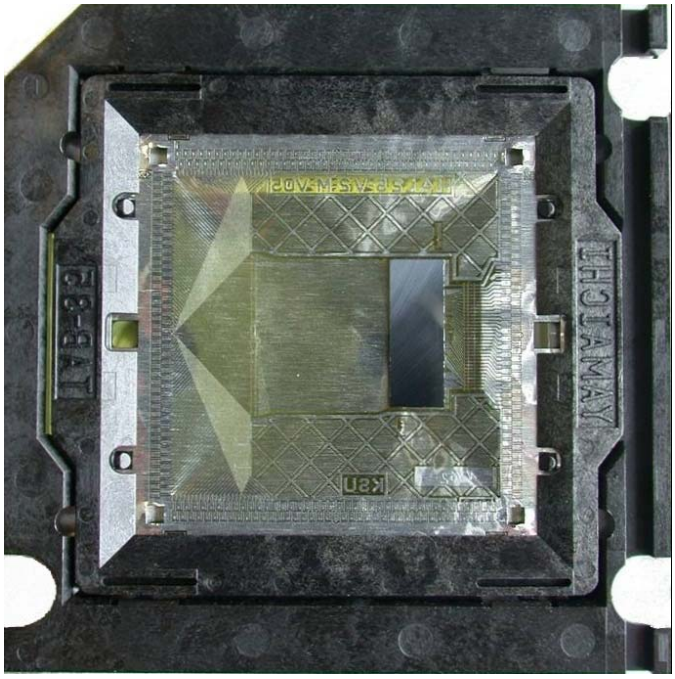

Figure 7: Framed (HAL25) chip.

Resulting from the experience gained in the use of this system in the production of the STAR silicon strip modules in Strasbourg, a number of additional features have been included to increase testability and reliability:

- Four eight-bit testpatterns are integrated in the cable layout, these are checked and give initial information about positioning and contact reliability: if this go/no-go test fails, positioning and possible contact contamination has to be checked first (red-yellow pad groups).

* See web version for coloured figures.

- The three types of cables, First, Middle and Last, are coded in the layout (row of seven blue pads in the right lower corner of figure 6)
- The F and L cable contain a bias trace for connecting the detector. In figure 6 this is the upper black trace connecting the two black pads. This trace is checked for continuity in the same test as the test-patterns, if there is a break in the trace the cable is discarded.
- Chip input channel test

The chip input channel test makes use of the test-pulse generator inside the chip, which can be programmed to sequentially pulse all input channels. In the test set-up all 128 inputs can be grounded by means of low-leakage CMOS gates.
If the inputs are left open, running the test, one should see on the (serial) output of the chip one testpulse for each channel at the correct position. If there are two adjacent pulses at the same time this means that there is a short between two cable traces.
With the inputs grounded, the same sequence is done again. Now no pulse should be seen on the output. The appearance of a pulse signifies an open trace or a bad bond for that channel.
With the test set-up it is possible to check all functions of the chip at full (10 MHz) read-out speed.

III. Hybrid and Flex Design

For cooling reasons the hybrid stiffener is made of five-layer carbon-fibre material [6]. It is not possible to put electrical traces on this material with thin or thick film techniques. So it was decided to design the power and interconnecting bus as a polyimide/aluminium cable (the flex) and glue this on to the stiffener. In this way a very low mass hybrid is realised (figure 8).

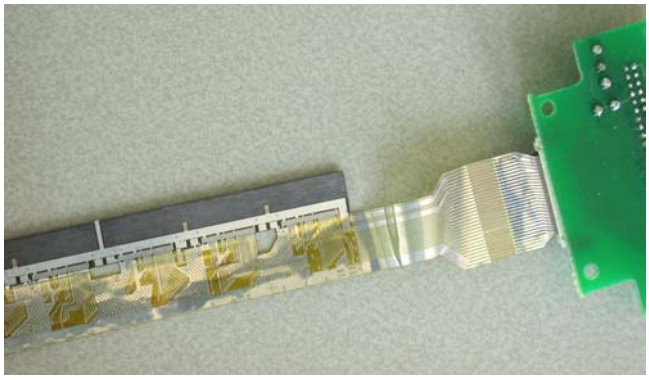

Figure 8: Hybrid with ZIF testboard.

The flex is a two-layer bus used for power, digital i/o and analog outputs. The interconnections between the two layers are made by bonded vias.
For this design the polyimide is 20 µm and the aluminium 30 µm thick.
In the SRTIIM institute electrical testing of flex assemblies is being researched and a first prototype for automated electrical testing has been developed.
The smd power decoupling capacitors and the 100 Ω LVDS terminations are soldered onto flex-mounts (very small special-purpose microcables with nickel solder pads) which are then bonded onto the flex. The advantages are that the flex does not have to undergo galvanic treatment to add solder pads and no soldering is needed to place the smd components on the glued flex-stiffener assembly. Only the output tail of the flex will have a soldering area.
In the flex layout there are six rows of bondpads with 250 µm pitch to connect the output side of the six chipcables to the flex.
The output tail of the flex has a removable test part which fits into a Zero Insertion Force (ZIF) connector testboard. At the other end, the flex includes a test pad pattern to facilitate checking all bus connections in the flex for shorts or breaks, using the ZIF pc-board and probes on the test pads.
After mounting of the chips, the ZIF connection is also used to test the full functionality of the hybrid. As a last step, the rear ZIF test part is removed and the flex tail is soldered to the laddercable. This is done with an automated thermode soldering system. All 24 connections are soldered with very high reliability in a few seconds in a single operation. Together with the research department of Unitek-Eapro, a company specialised in electronic assembly products which produces these machines for industry, this technique was successfully adapted to aluminium microcables.
An important change compared to the traditional copper trace soldering is that with aluminium traces sufficient spill-over area's covered with nickel/solder must be created to prevent the forming of solder bridges between traces.
This soldering system was chosen because connecting of the laddercables is the final module assembly step. It is also the only system which, in case of failure, can be redone. The reason for doing this as a final step, is that two hybrids have to be bonded to a double side silicon detector. Transport and handling during this bonding operation and the positioning of completed modules on the ladder assembly machine becomes very complicated and dangerous if there are already two laddercables connected to it.

IV. Laddercable Design

The laddercable is the connection between the modules on the ladder and the endcapmodules which are mounted at the end of the ladders. Ladders are read out from both sides to keep laddercable length within reasonable limits. A talk on the endcaps and ASIC's used in their design has been given at the Stockholm LHC workshop [7].

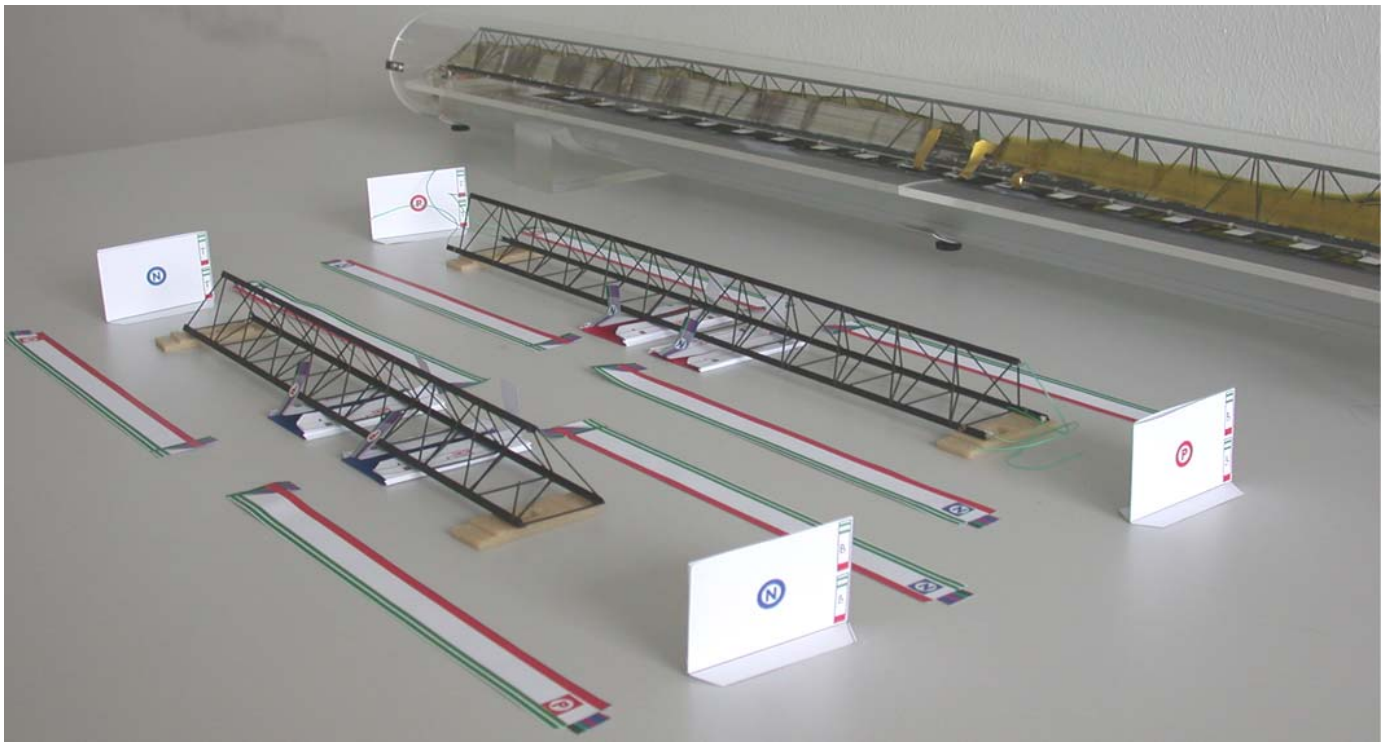

Figure 9: Ladder cabling layout.

The laddercables are routed along the ladder structure in parallel, so at the endcap there are up to 13 cables on top of each other (figure 9). The length of the cables varies from eight cm to 60 cm depending on module position. For this reason, laddercable assemblies consist of two parts: the long (8-60 cm) ladderstripe and a short laddertail, which is bonded perpendicular on to the ladderstripe. The latter is soldered to the output tail of the flex. The width of the laddercable is 23.5 mm.

The laddercable has traces for power supply, detector bias supply, CMOS JTAG control signals, LVDS readout signals and analog output signals.

Because the chips use 2.5V supply voltage, these traces have been designed for very low voltage drop, i.e. low series resistance, approximately 0.1 Ω for the 60 cm cable. Signal trace series resistance is around 1 Ω, trace width is 300 µm.

The LVDS signals and analog outputs are differential signals, which should be terminated with approximately 100 Ω. Also the analog signal lines must have very low cross-talk. For this reason these lines have been placed between two wide ground traces and laddercables are mounted in high or low positions shifted so much that the analog lines of each cable are shielded between the ground traces of neighbouring cables. Position is determined by the two holes in the mounting tabs, which is used to fixate the cable (figure 10).

In this way the analog traces form a differential strip-line with ground shields on both sides with very little cross-talk. Furthermore the ground traces have the same width, so any edge-induced interference from these traces to the analog lines due to current variations is common mode and mostly rejected.

To attain the required impedance of 100 Ω, a very low density polyimide foam, TEEK, developed by NASA and the Japanese Unitika company is used as a spacer material between the cables. This foam is 300 µm thick and has a dielectric constant of 1.02, which also helps to increase the impedance. It will be attached to the cables using a 45 µm transferable gluefilm.

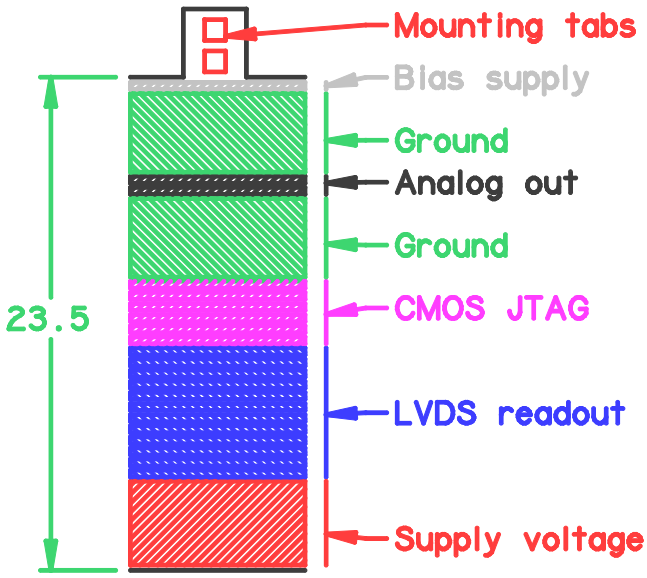

Figure 10: Ladder cable design.

V. Conclusion

Aluminium microcable technology is very useful for the design of low mass complex assemblies like silicon tracker front-end modules. It gives an extra degree of freedom compared to traditional wire bonding. Not only can one design in three dimensions, but some relative movement between bonded components is allowed.

Another advantage is the possibility to produce sub-assemblies like chips with chipcables, that can be tested simply and quickly for full functionality at high read-out speeds without the need of complex set-ups like probe stations, etc.

Industry has proven to be able to produce prototype sub-assemblies and modules.

We foresee to produce and test these sub-assemblies and modules partly in the concerned institutes, partly in industry.

VI. Acknowledgements

We are indebted to R. Vermeulen and P. van der Heiden of Unitek-Eapro Helmond (NL) for the use of their facilities and their assistance with the thermode soldering process and to Y. Echigo of Unitika Japan for donating samples of their TEEK polyimide foam.

References

[1] ALICE ITS Technical Design Report CERN/LHCC 99-12

[2] Proceedings of Seventh Workshop on Electronics for LHC Experiments CERN/LHC 2001-034: Christine Hu-Guo et al: The HAL25 front-end chip for the ALICE silicon strip detectors, page 76-80.

[3] Proceedings of Fifth Workshop on Electronics for LHC experiments CERN/LHC 99-33: J.R. Lutz et al: Tab Bonded SSD Module for the Star and ALICE trackers, page 147-151

[4] Proceedings of Fifth Workshop on electronics for LHC experiments CERN/LHC 99-33: A.P. de Haas et al: Very low mass cables for the ALICE silicon strip detector, page 143-146

[5] Proceedings of Fourth Workshop on Electronics for LHC Experiments CERN/LHC 98-36:
S. Bouvier et al: TAB packaging technology for the Si-strip front-end detector assembly, page 511-513.

[6] Proceedings of Seventh Workshop on Electronics for LHC experiments CERN/LHC 2001-034: G. Feofilov et al: conductive cooling of SDD and SSD front-end chips for ALICE, page 368-372.

[7] Proceedings of Seventh Workshop on Electronics for LHC experiments CERN/LHC 2001-034: R Kluit et al: Design of endcap electronics for the ALICE ITS SSD, page 47-51.