Radiation-Hard ASICs for Optical Data Transmission in the ATLAS Pixel Detector

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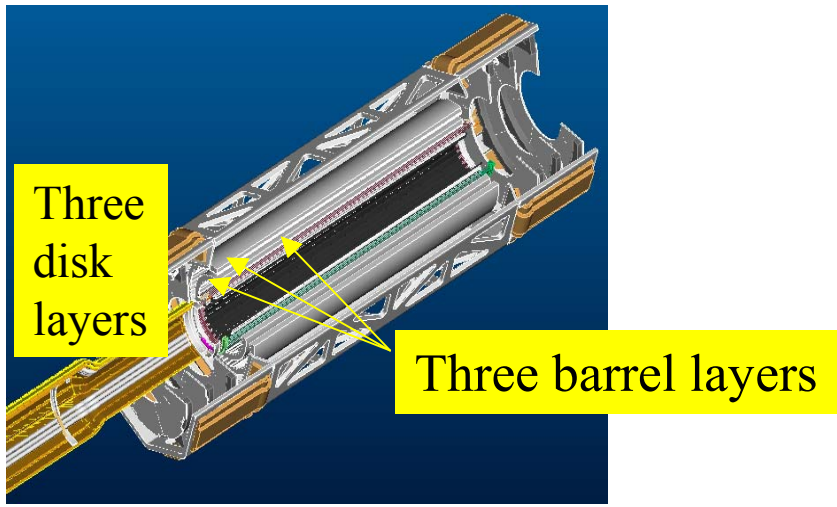
Outline

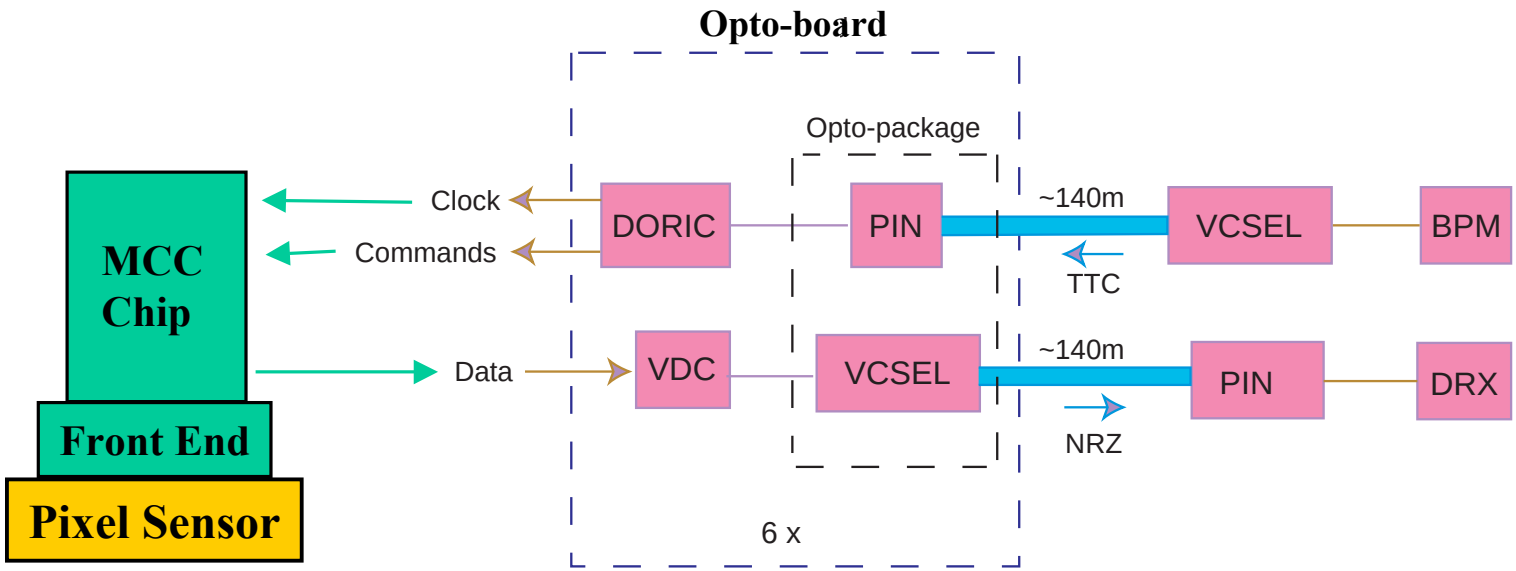
- Introduction
- Results from IBM 0.25µm Submissions
- IBM 0.25µm Irradiation Results
- ASIC Testing Station
- Summary & Outlook

ATLAS Pixel Detector



- **Inner most tracking detector**
- **~ 100 million channels**
- **3 layers with radii 12.25 cm, 9.85 cm and 5.05 cm in the barrel**
- **Radiation doses at radius of the middle layer in 10 years of LHC operation:**
- **~ 10^{15} 1-MeV n_{eq}/cm^2; Total dose: 50 Mrad, Opto: ~ 30 Mrad**

ATLAS Pixel Electronics Readout Path



VCSEL: **Vertical Cavity Surface Emitting Laser diode** ✓

VDC: **VCSEL Driver Circuit**

PIN: **PiN diode** ✓

DORIC: **Digital Optical Receiver Integrated Circuit**

Radiation Hardness of PINs and VCSELs

PIN:

- Responsivity drops to ~ 2/3 after irradiation to lifetime dose (0.5 → 0.3 mA/mW)
- Lifetime test shows no failures
- Rise & fall times unchanged for $V_{bias} > 5V$

VCSEL:

- After 4×10^{15} n/cm^2, annealing at 20mA restores 100% of original light output

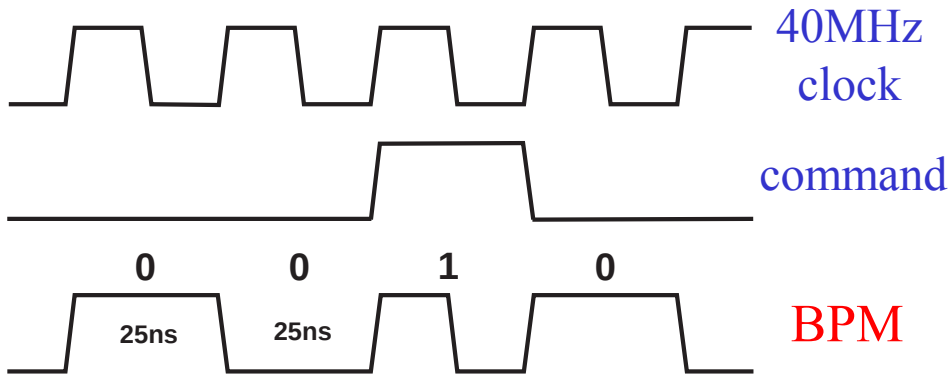
⇨ Anneal VCSELs during irradiation study of optical links!

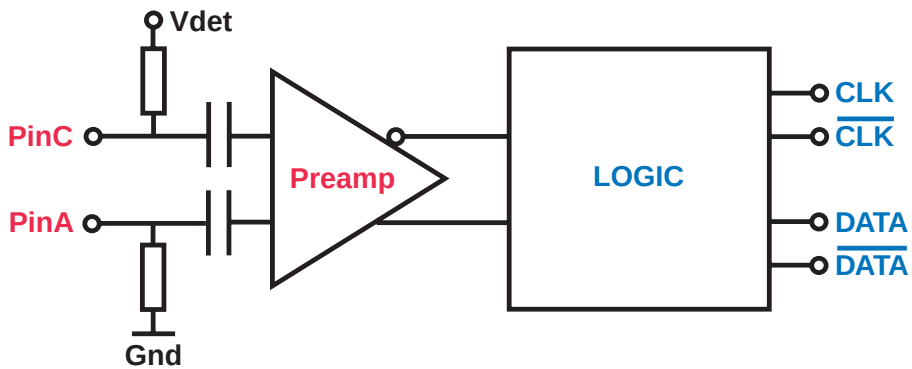
VCSEL Driver Circuit Specs

- Convert LVDS input signal into single-ended signal appropriate to drive VCSEL diode
- Output current: 0 to 20mA, controlled by external voltage
- Standing current: ~1mA to improve switching speed
- Rise & fall times: 1ns nominal (80MHz signals)
- Duty cycle: 50% +/- 4%
- "On" voltage of VCSEL: up to 2.3V at 20mA
- Constant current consumption!

Digital Optical Receiver IC Specs

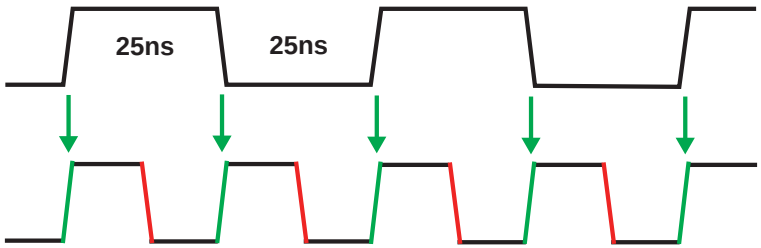
- Decode Bi-Phase Mark encoded (BPM) clock and command signals from PIN diode
- Input signal step size:
  40μA to 600μA
- Extract 40MHz clock
- Duty cycle: 50% +/- 4%
- Total timing error: < 1ns
- Bit Error Rate (BER):
  $< 10^{-11}$ at end of life





DORIC Logic

- Training period: ~25µs



Data = "0" : 20MHz clock

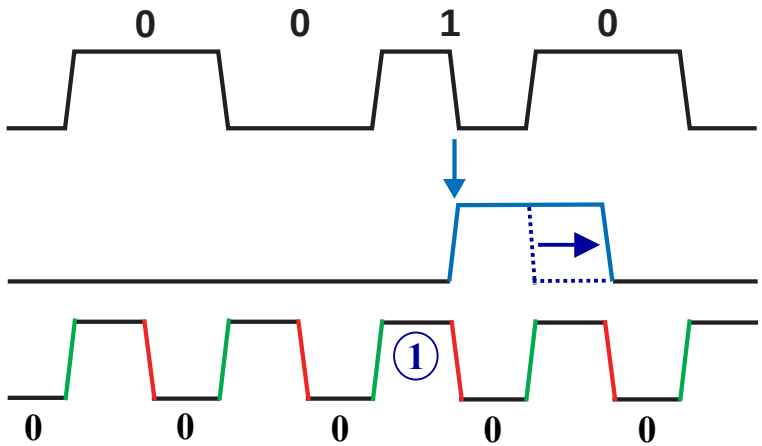
Leading edges ⇦ Input transitions

Trailing edges ⇦ internal delays

Delay of Trailing Edges → 40MHz Recovered Clock

Delay Locked Loop:
Duty Cycle = 50% ?

⇨ Ready for data:



VDC & DORIC Design History

- **Original design by ATLAS SemiConductor Tracker (SCT) team: AMS 0.8μm BiPolar in radiation tolerant process, 4V**

- **DMILL #1-3: Summer 1999 - May 2001**
  0.8μm CMOS, rad-hard, 3.2V

  VDC & DORIC: #3 meet original electrical specs

  April 2001 Irradiation: severe degradation of circuit performance!

  Not radiation hard enough for ATLAS pixel optical link

⇨ **Migrate to IBM 0.25μm: Summer 2001, 2.5V**

Enclosed layout transistors and guard rings for improved radiation hardness

VDC & DORIC Designs in 0.25µm

- **IBM #1-2: June - October 2001**
  - **VDC:** decouple adjustment of bright & dim currents
    more constant current consumption
  - **DORIC:** optimized differential preamp circuit
    ⇨ both circuits meet original specs
- **IBM #3: November 2001**
  - **VDC:** further improvements to current consumption, 4-ch IC
  - **DORIC:** single ended preamp keeps PIN bias off chip
    improved delay control circuit, …
    ⇨ single ended preamp matches prior performance

→ Results

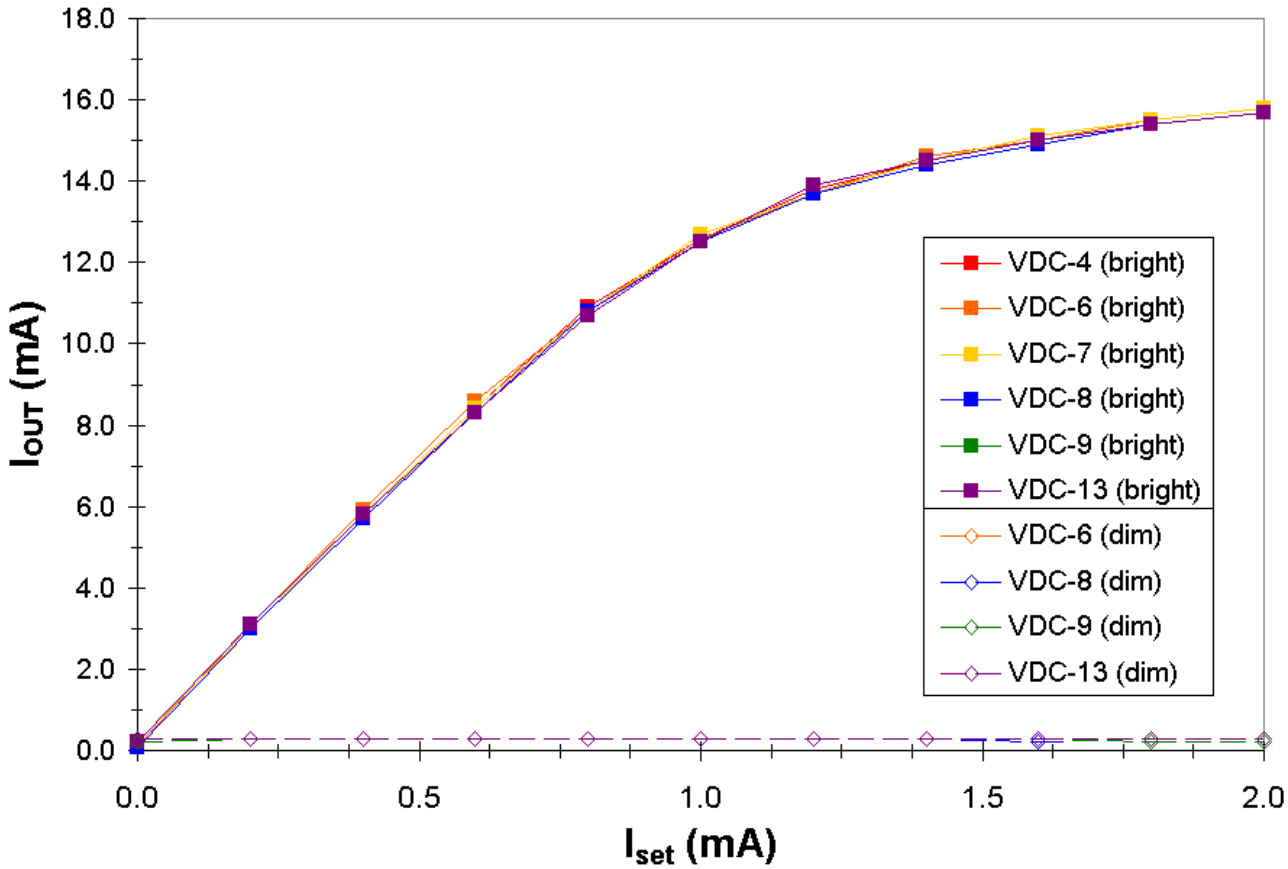
- **IBM #4: April 2002**
  - **VDC:** compatible with common cathode VCSEL arrays, 4-ch IC
    ⇨ need to improve switching speed of pFETs

→ Results + Irrad.

  - **DORIC:** preamp optimized for common anode PIN arrays
    improved delay control circuit: centers clock at 50% duty cycle
    reset added for slow and controlled recovery, …, 4-ch IC
    ⇨ improved performance over #3
    ⇨ need to be compatible with common cathode PIN arrays!

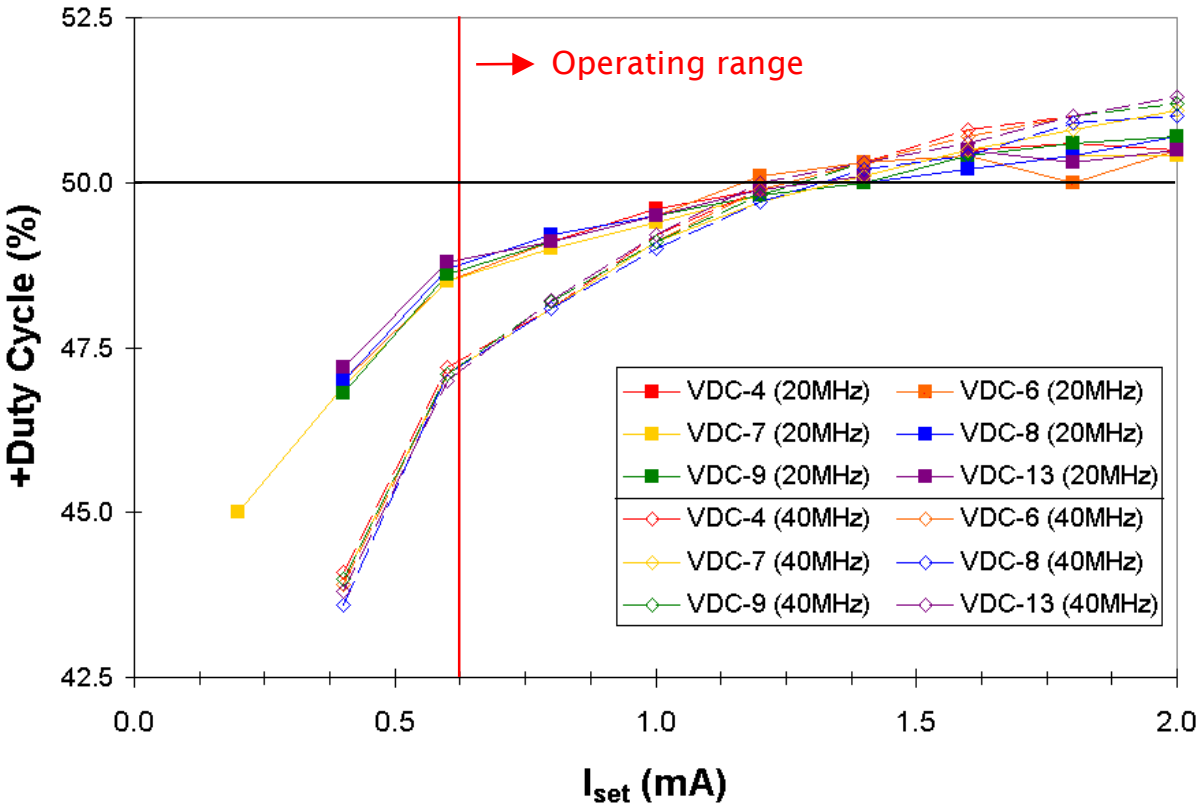
→ Results + Irrad.

VDC-I4 Results: VCSEL Current vs. I_{set}



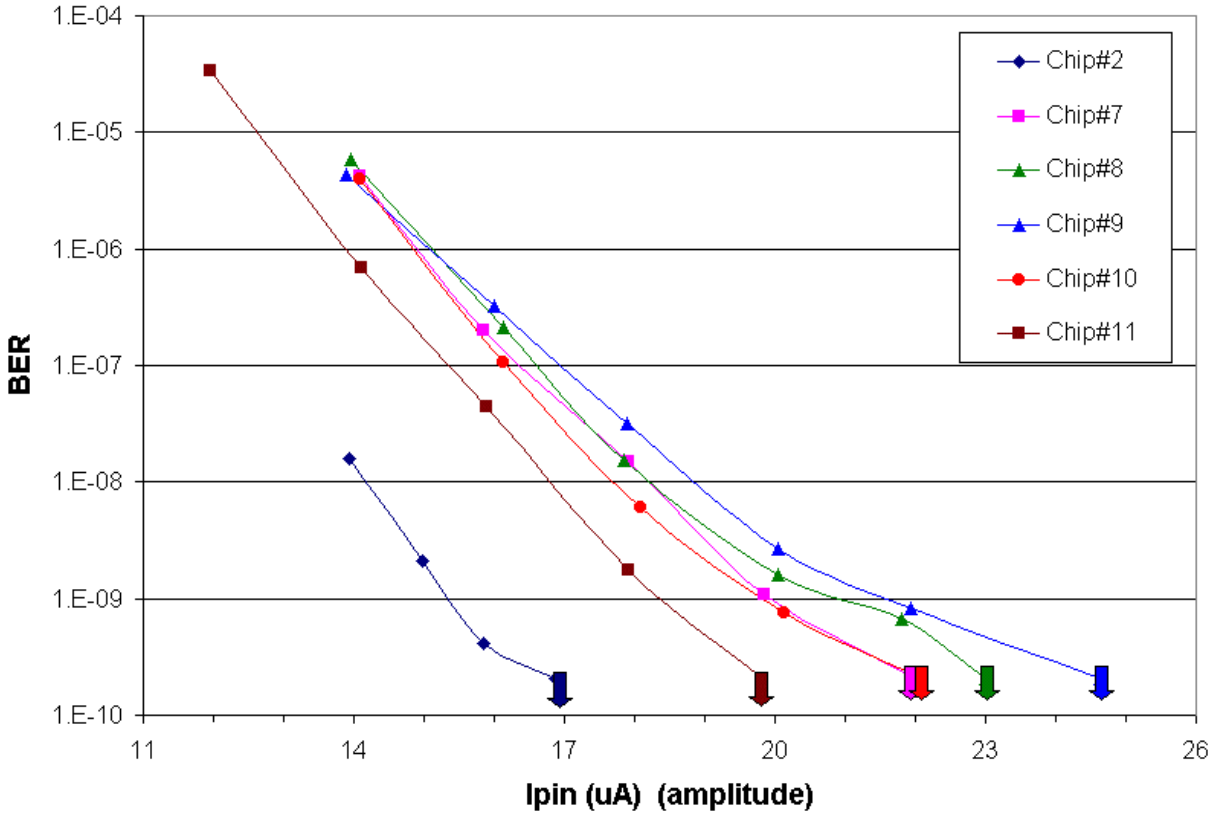
- 10 Ω in series with VCSEL ⇨ early saturation at high I_{set}
- Need to increase I_{bright} (VDC-I3 reached 20mA), I_{dim} (~1mA)

VDC-I4 Results: Duty Cycle



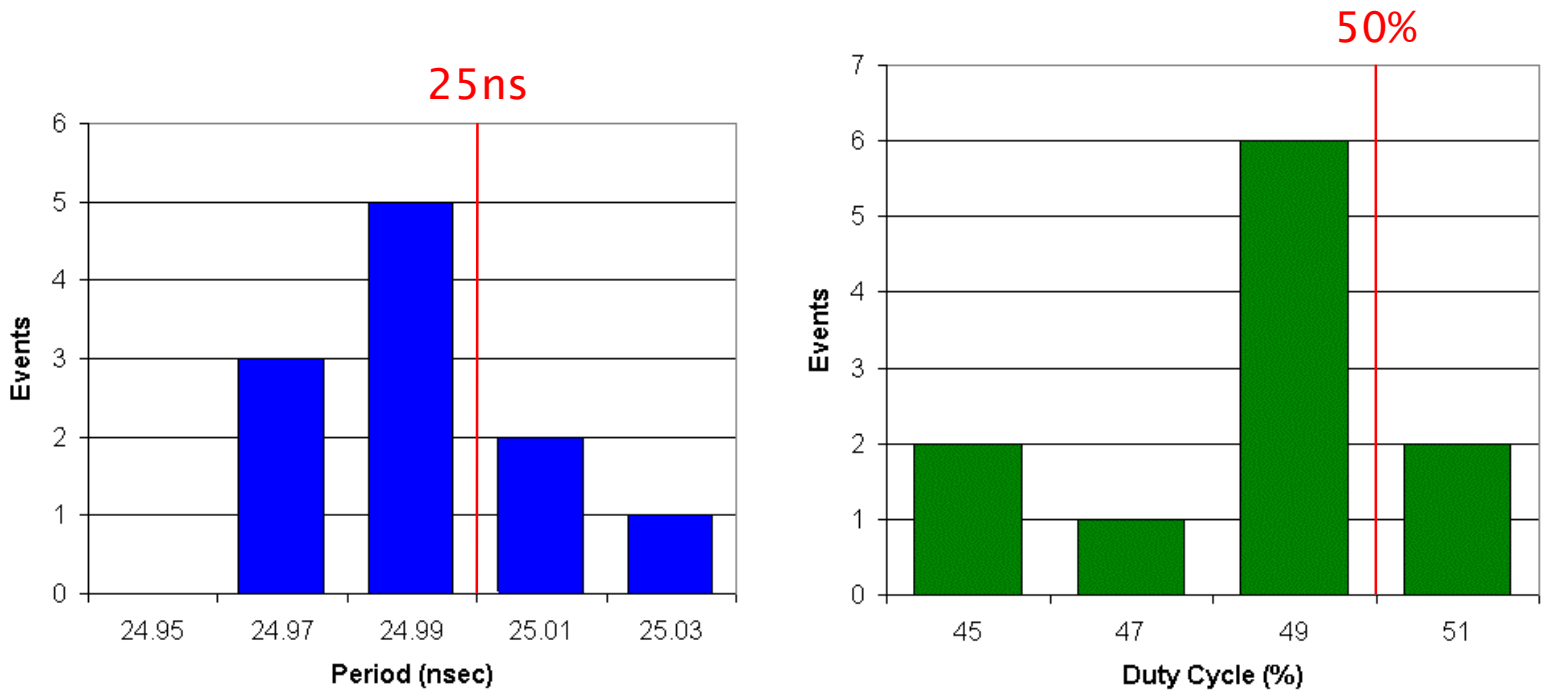
- Balanced current consumption
- Rise & Fall times: 1.0...1.4ns over operating range
  - ⇨ improve speed of pFETs (common cathode design)

DORIC-I3: Bit Error Rate vs. I_{PIN}



- PIN current thresholds for no bit errors: 20…25μA
- DORIC-I4: improved performance (< 20μA)

DORIC-I3: Duty Cycle of Decoded Clock

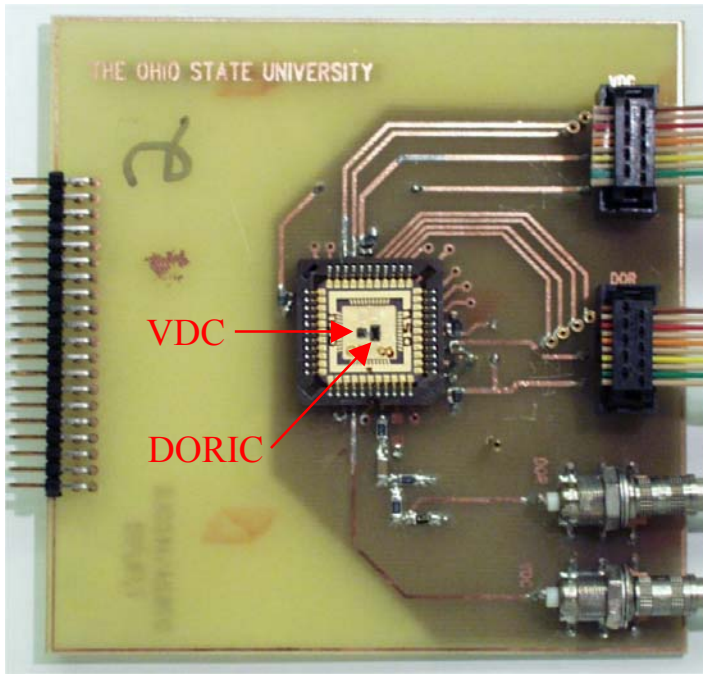


- 9 out of 11 DORIC-I3 within spec: 46…54%
- DORIC-I4:
  - duty cycle centered at 50%
  - slow reset works
  - various improvements are successful

Irradiation of VDC-I4 & DORIC-I4, Aug. 2002

- 24 GeV proton test beam at CERN (T7)
- Cold box: electrical testing of single channel VDC & DORIC
- Shuttle system: testing of optical links on opto-board, 4-channel VDC & DORIC

Cold box test board



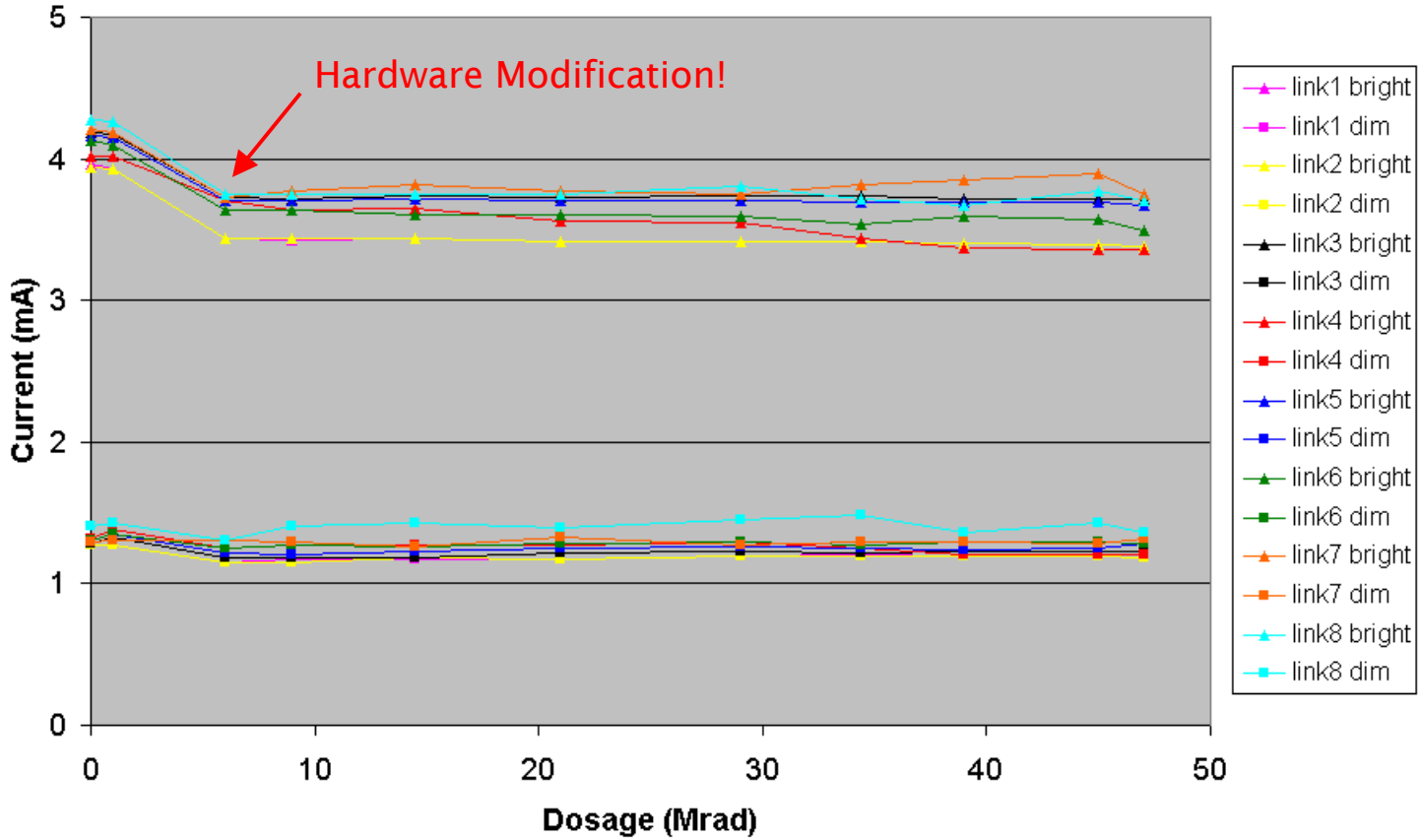
PRELIMINARY RESULTS ⇨

DORIC-I4: Bit Error Threshold vs. Dosage

PIN current thresholds for no bit errors:

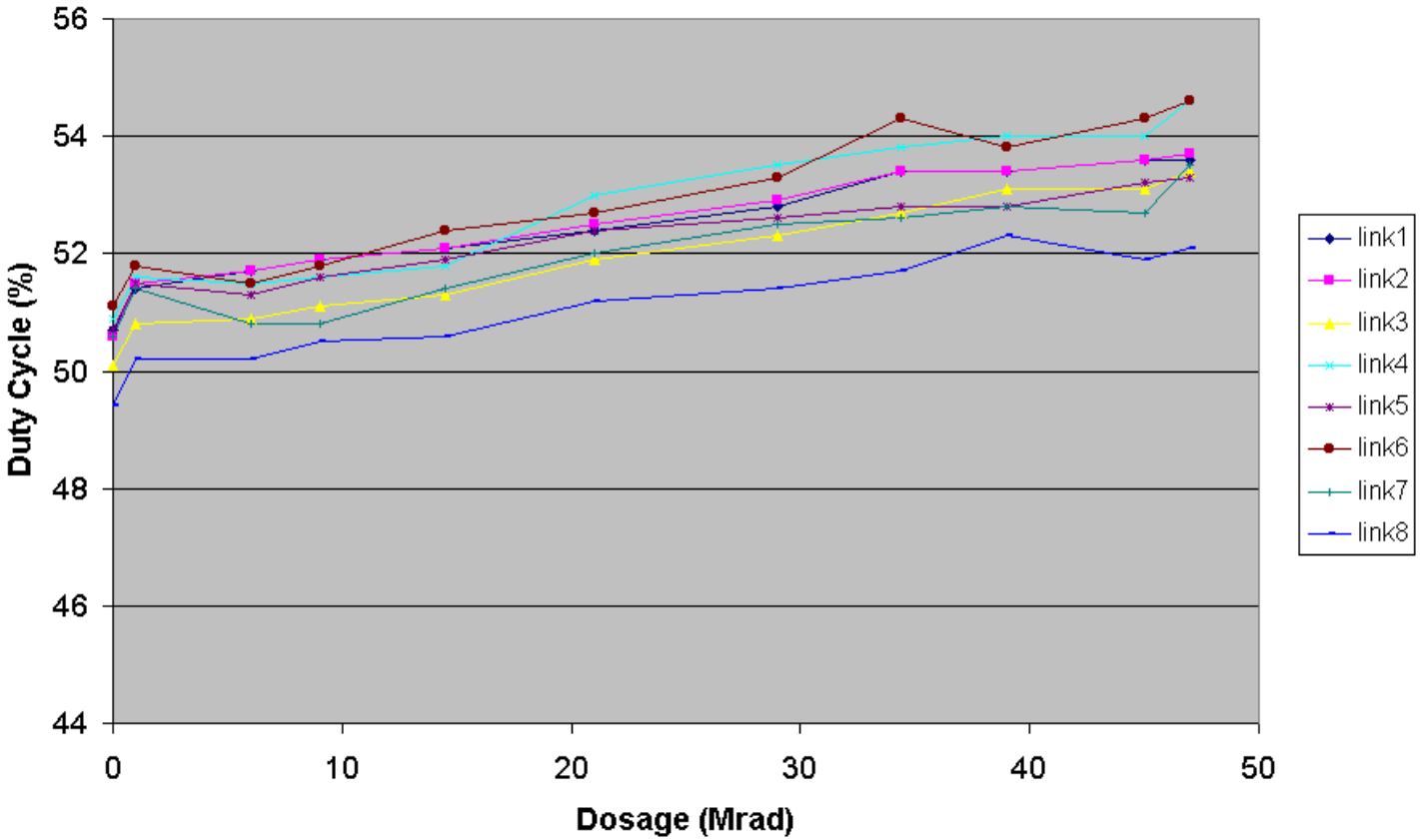
- ~ 12μA for all 10 tested DORIC-I4 circuits
- constant up to 45Mrad for all tested chips

VDC-I4: VCSEL Current vs. Dosage



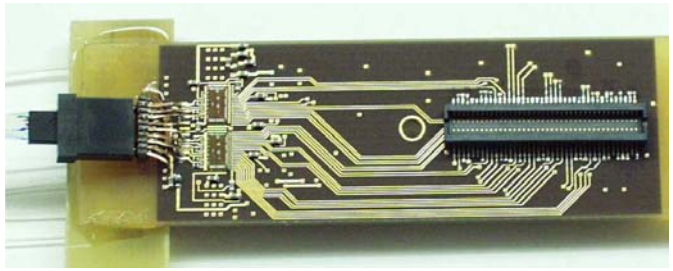
- Bright & dim currents constant up to 45 Mrad

VDC-I4: Duty Cycle vs. Dosage



- Duty cycle of VDC-I4 increases by ~ 2% after 45 Mrad

Test Boards for Irradiation in Shuttle



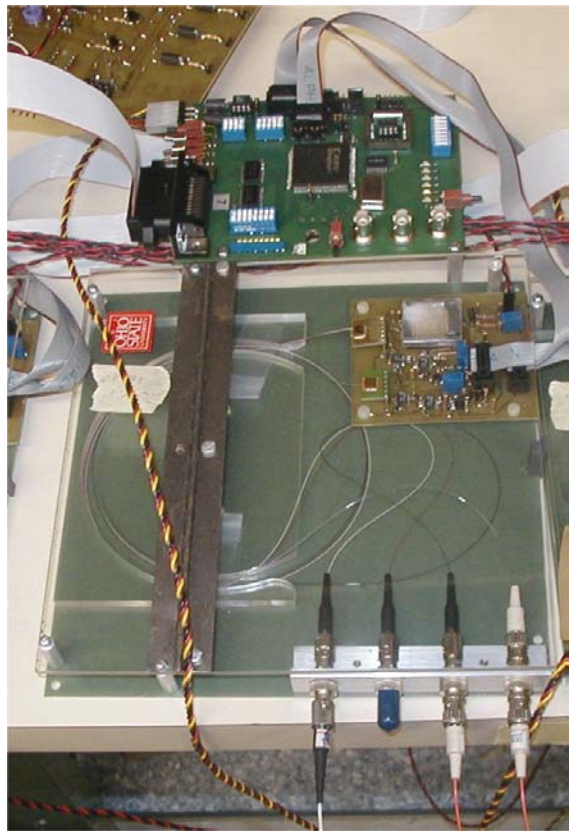
Opto-board with 7 opto-links

Bi-phase marked optical signal

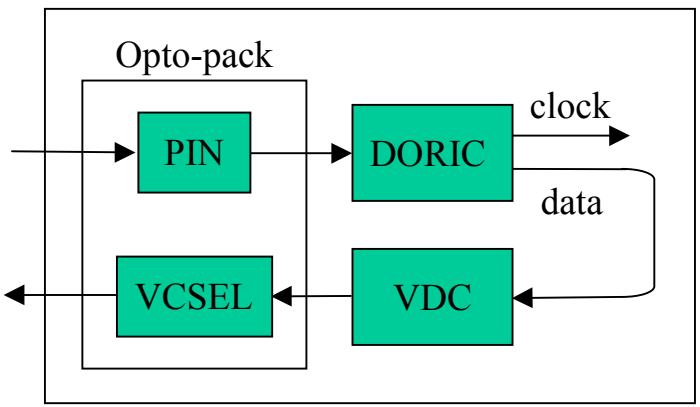
25 m fibers/wires

Decoded data

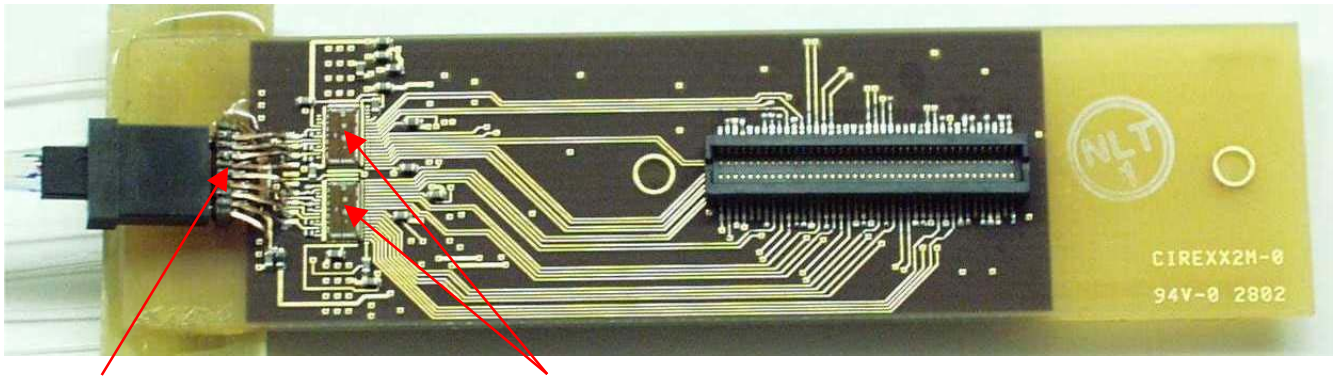
Bit error test boards in control room (one per opto-link)

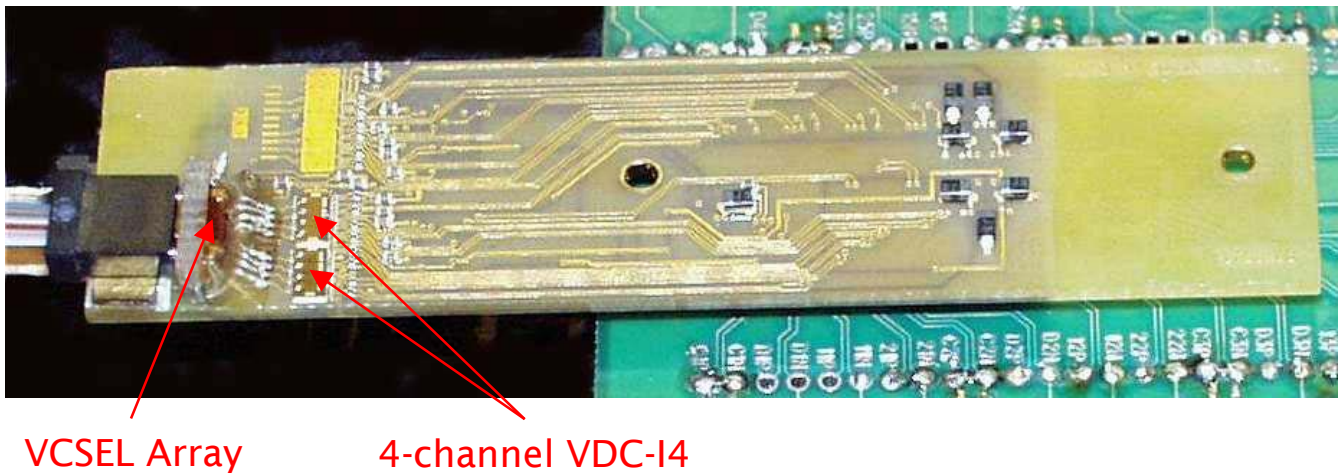


Opto-link



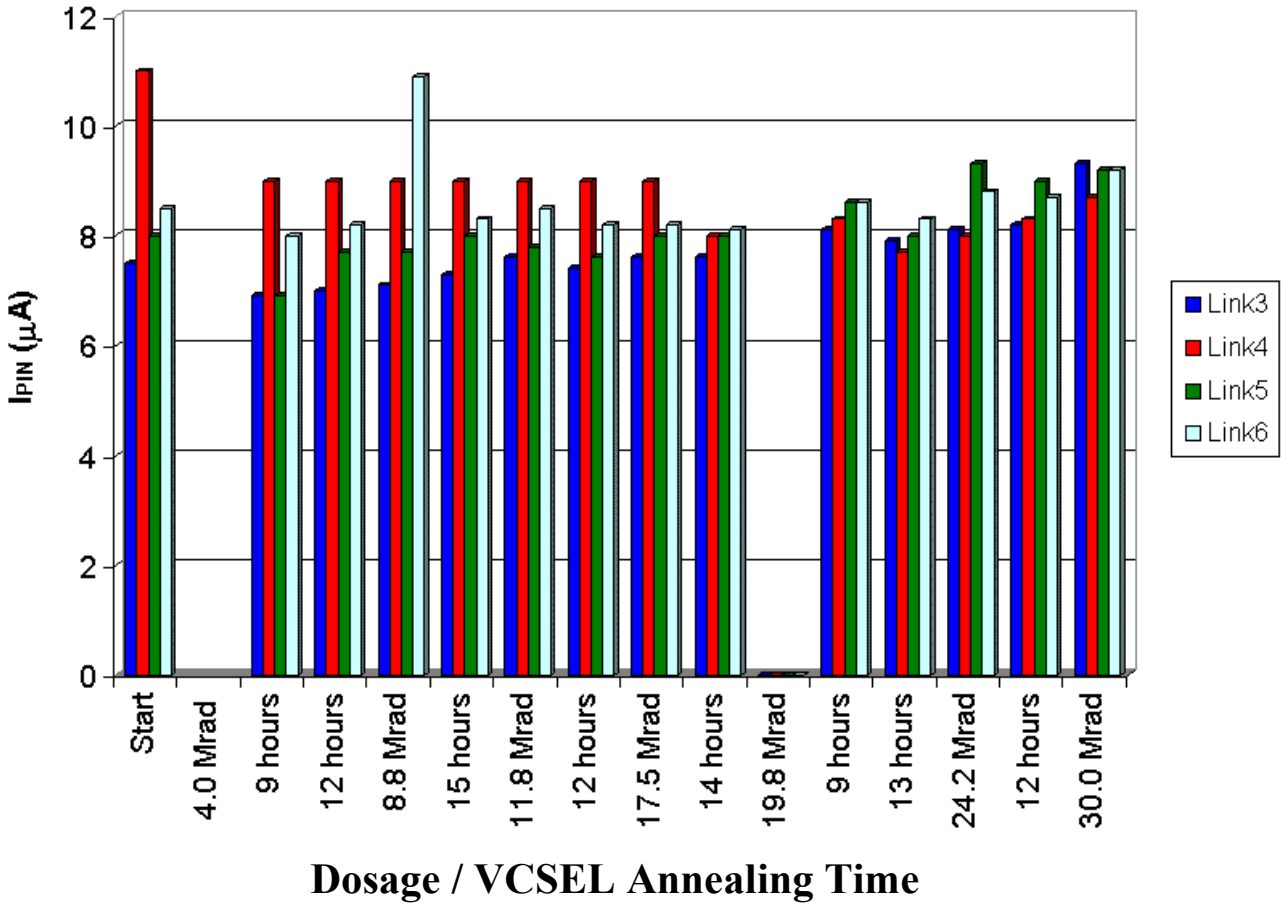
Opto-Board for Irradiation Study





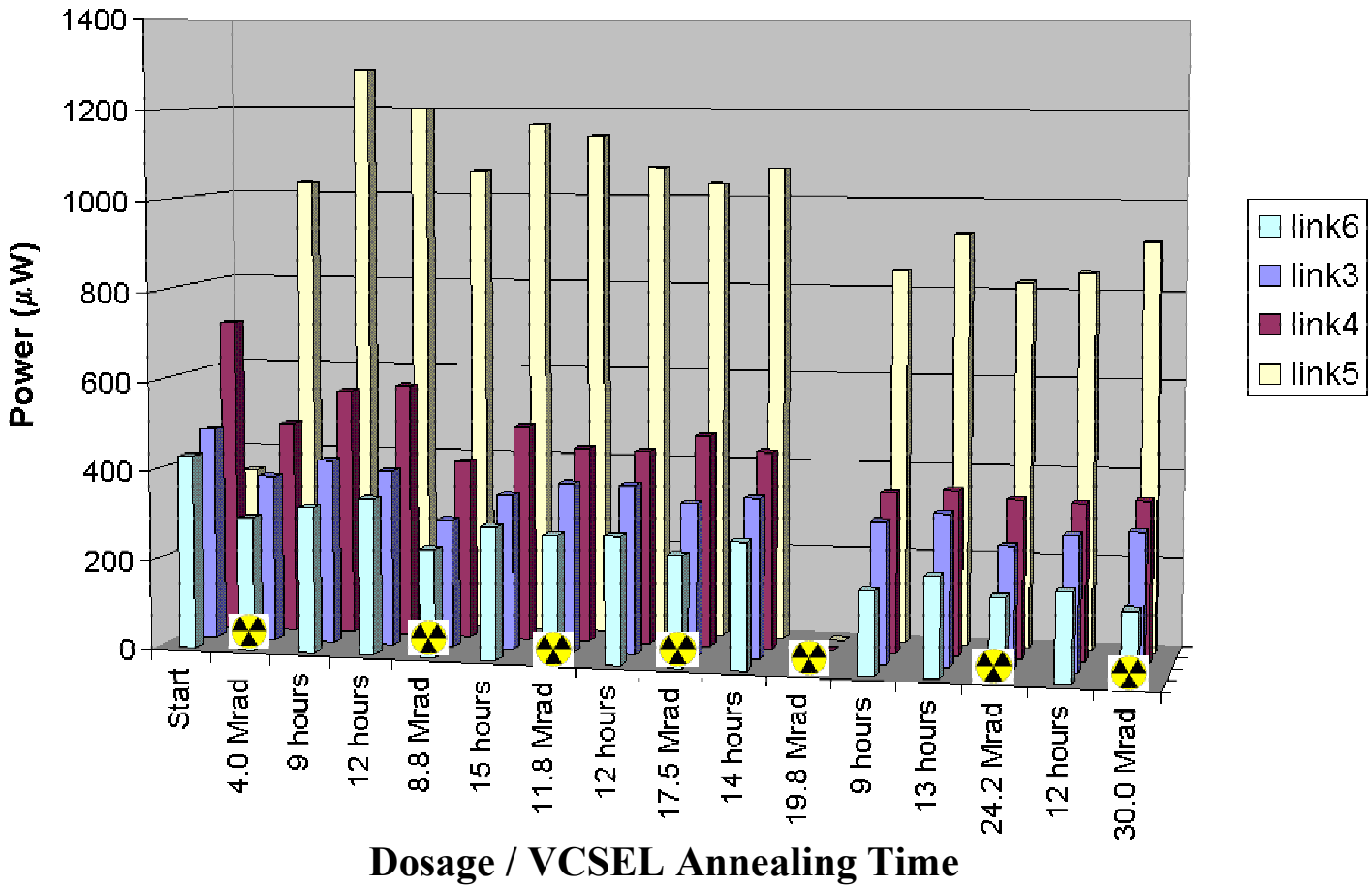
- Two 4-ch DORICs, four 4-ch VDCs on fully populated board

Opto-Board Bit Error Threshold vs. Dosage



- VCSELs annealed with 20mA during indicated periods
- Bit error threshold remains ~ constant up to 30Mrad

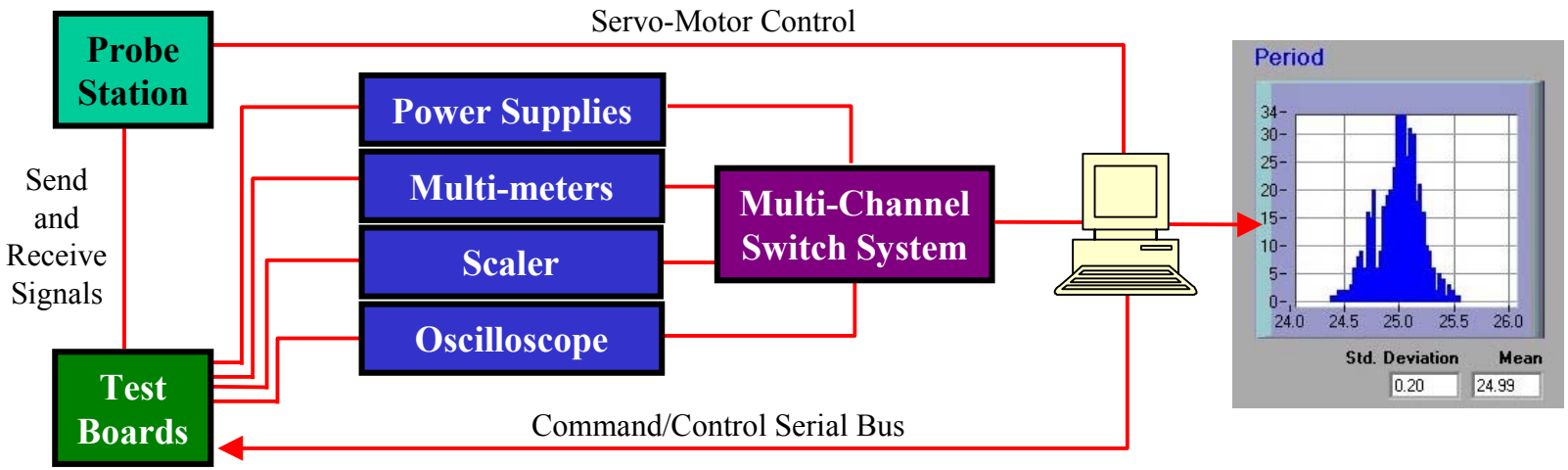
Opto-Board Optical Power vs. Dosage



- Optical power decreases by < 50% after 30Mrad
  - ⇨ Complete optical link is adequately radiation hard

ASIC Testing

- **DMILL #1 - IBM #2:**
  - **OSU-designed stand-alone BER & irradiation test boards used**
  - **Testing done manually with oscilloscope, multi-meters, etc.**
- **IBM #3 and beyond:**
  - **Automation using NI LabView implemented**
  - **Stand-alone test-boards redesigned for use with computer interface**
  - **Probe-card with Lab View interface implemented for testing bare dice**
    - ⇨ **continual monitoring of tests for long periods (ie: irradiation)**
    - ⇨ **large statistical samples of measurements possible**
    - ⇨ **makes mass testing of ASICs feasible (1000's of dice to test!)**



Summary & Outlook

- VDC-I4 & DORIC-I4 (IBM 0.25μm) meet specs
- Radiation hardness of VDC-I4 & DORIC-I4 (IBM 0.25μm) appears adequate for pixel system:

  Circuits continue to perform well after 30-45Mrad!
- Automated testing station has been implemented
- Next submission: Nov./Dec. 2002
  - Improve speed & ampl. of common cathode VDC
  - Implement common cathode preamp in DORIC, tune preamp: dynamic range, S/N, etc.