Test and Evaluation of HAL25:
The ALICE SSD Front-End Chip

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Abstract

HAL25 is a mixed low noise, low power consumption and radiation hardened ASIC intended for the Silicon Strip Detectors (SSD) read out in the ALICE tracker. It is designed in a 0.25 micron CMOS process.

It contains 128 analogue channels, consisting each of a preamplifier, a shaper and a storage capacitor. The analogue data is sampled by an external logic signal and then is serially read out through an analogue multiplexer. This voltage signal is converted into a differential current signal by a differential linearised transconductance output buffer. A slow control mechanism based on the JTAG protocol is implemented for a programmable bias generator, an internal test pulse system and functional modes selection.

This paper presents HAL25_V2 measurement results. Features related to new requirements, like the maximum readout frequency and higher input rate, are also discussed.

Introduction

HAL25 is a mixed, analogue digital ASIC designed for the read-out of Silicon Strip Detectors (SSD) in the ALICE tracker. It is designed with special radiation tolerant design techniques [1] in a commercial 0.25 micron CMOS process to meet the requirements of low noise, low power consumption and radiation hardness.

HAL25 contains 128 analogue channels, consisting each of a preamplifier, a shaper and a capacitor to store the voltage signal proportional to the collected charge on a strip of a silicon detector. The input dynamic range is ± 14 MIPs with a good linearity and the peaking time is adjustable from 1.4 to 2.2 µs. The data is sampled by an external logic signal and is read out through an analogue multiplexer. This voltage signal is converted into a differential current signal by a differential linearised transconductance output buffer. The chip is programmable via the JTAG protocol, which allows to:

- Set up a programmable bias generator which tunes the parameters of the analogue chains;
- Set the so called "transparent mode" to characterise one specific channel;
- Check analogue behaviour of the chip by injecting adjustable charges to the input of selected channels with a programmable pulse generator;
- Perform the boundary scans.

An internal current reference source is adjustable in 5 steps by the JTAG controller in order to compensate process variation. Registers designed with majority vote logic prevent the Single Event Upset (SEU).

Two versions of HAL25 have been produced. Delivered in July 2001, the HAL25_V1 was found to demonstrate good performances in all aspects of the design except yield. The HAL25_V2 is intended to increase the yield. New front-end solution allows, for the same dynamic range, a higher overall gain thus the higher S/N ratio.

This paper presents HAL25_V2 results. They are obtained from measurements on probed chips (bare or on wafer) and bonded chips. Features related to new requirements, like the maximum readout frequency and higher input rate, are also discussed.

HAL25_V2 Design

As explained in a previous publication [2], HAL25 contains 128 analogue channels. Each channel has a charge preamplifier followed by a shaper with an adjustable peaking time from 1.4 to 2.2 µs. In a new design, the adjustable feed back resistor in the shaper is replaced by a linearised source degenerated differential pair (Fig. 1a) to meet requirements of large dynamic with good linearity specifications. The front-end amplifier allows an input dynamic range (±14MIPs) with an excellent linearity (Linearity error < 4%). The typical voltage gain of the front-end amplifier is 50 mV/MIP. This solution does not need an inverter-switch circuitry for different input polarities, and improves the power consumption budget. We can set V_{DC} to different values for different input polarities in order to make use of the maximum dynamic range in the shaper (Fig. 1b). The transconductance of the feedback circuit depends on the

bias current in the differential pair. It can be tuned by changing this current. It makes the peaking time adjustable in the shaper.
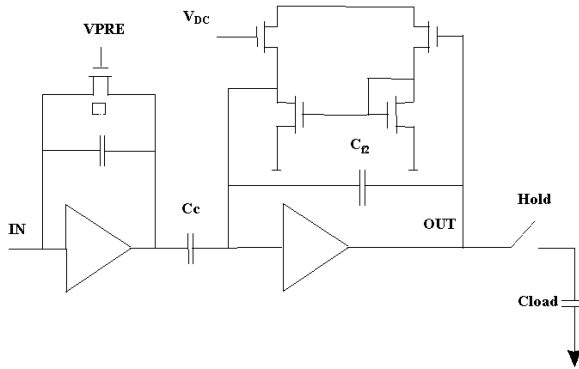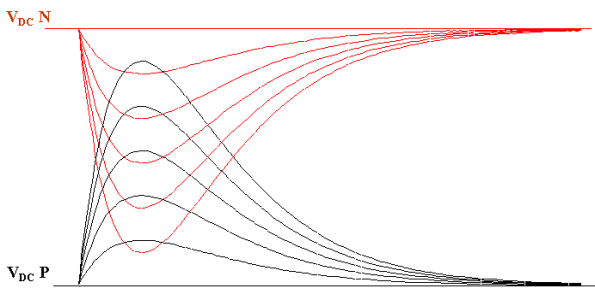

Fig. 1a Front-End amplifier

Fig. 1b Different bias V_{DC} for different input polarity

The signal at the output of the shaper is sampled by an external logic signal (Trigger) and stored on a capacitor. The data is serially readout by a 128:1 analogue multiplexer at the nominal readout frequency of 10 MHz. The voltage data is converted to current by a differential current buffer.
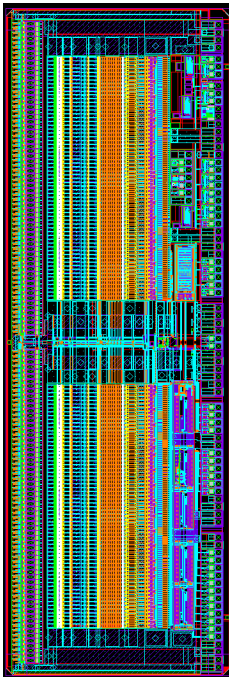

Fig.2 Chip Layout

Figure 2 shows the layout of HAL25. The 128 analogue chains are split into two 64 channels groups. Power is provided from top, middle and bottom backend pads in order to reduce voltage drop in metallisation resistance. All the pads except the power supply pads are protected with diodes. Pads used by the JTAG protocol are CMOS level while the readout control pads comply with the LVDS standard. The I/O pads, especially the detector input pads, are designed to be compatible with micro-cable bonding techniques such as the Tape Automated Bonding. The present TAB pitch of 80 μm leads to chip dimensions of 11.9 mm from top to bottom and 3.65 mm from front to back edge.

HAL25_V2 Performance

A. Pedestal distribution, Gain and linearity

Figure 3 shows the pedestal distribution of the 128 channels from one chip. The standard deviation of the Gaussien fit is 34 μA, which is sixth of 1MIP signal.
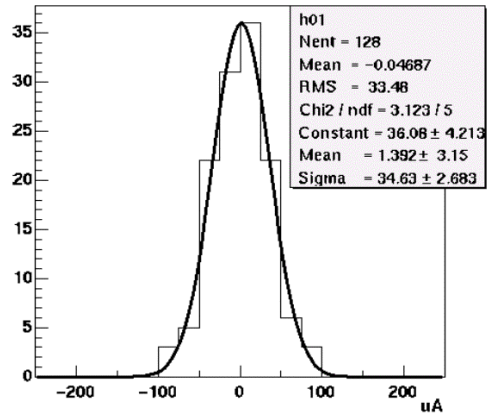

Fig. 3 Pedestal distribution of 128 channels

Figure 4 shows an output stream of a chip from channel 1 to channel 128. A 1 MIP signal injected on one channel shows up clearly after the pedestal subtraction in the channels.
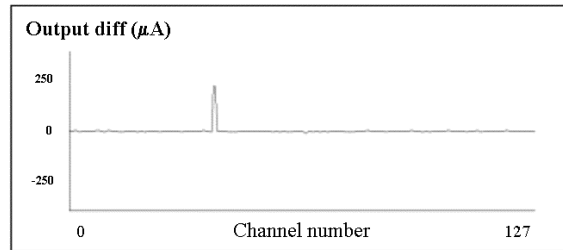

Fig. 4 Output stream

HAL25 has a nominal current gain of 220 μA/MIP which is tuneable by changing the bias current of the differential current output buffer. The simulation curve fits well with measurements and looks like an ideal CRRC shape as shown in figure 5. The linearity error is smaller than 2.5% in the signal range of ±10 MIPs (Fig. 6) and smaller than 4% for signal up to ±14 MIPs. Figures 5 and 6 show measurements on a channel.
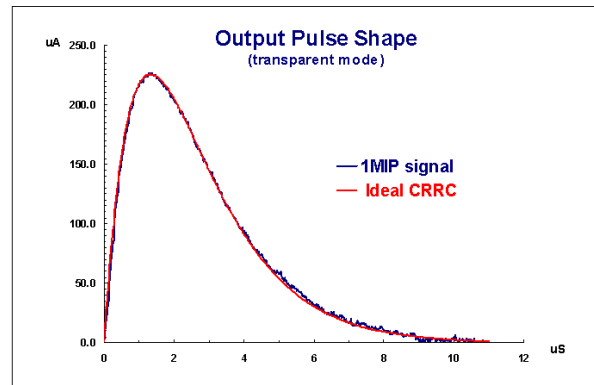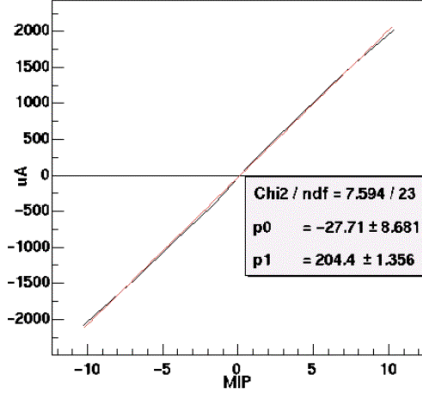

Fig. 5 Output pulse shape

Fig. 6 HAL25 linearity

Fig. 8 Noise distribution

B. Gain and Test Pulse Amplitude Uniformity

62 HAL25 circuits have been measured from two V2 wafers using the internal test pulse generators. A signal of about 8 MIPs has been injected into each channel. Figure 7 represents the output current pulse amplitudes.
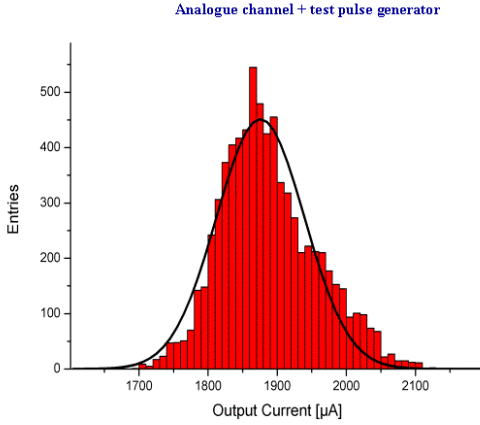

Fig. 7 Output amplitude uniformity

The average amplitude is near 1.9 mA with a standard deviation of 63 μA. It shows a good uniformity both for the gain of the front-end amplifier and the amplitude of the test pulse generators.

C. Noise

Figure 8 shows a noise distribution of 128 channels. The small peak at the right hand of the fitted distribution curve corresponds to a tested channel, which is bonded to a PCB test board. It has an equivalent input capacitor of 1.5 pF.

The equivalent noise charge for 0 input capacitance is about 215 electrons with a standard deviation of 5 electrons. The measured slope of the equivalent noise charge as a function of the input detector capacitor is about 25 e^-/pF.
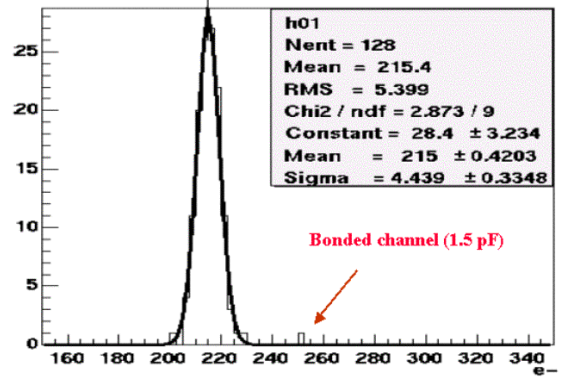
D. Maximum Readout Frequency

HAL25 is designed to be readout at 10 MHz. However for new requests, we have measured the chip with the readout frequency up to 30 MHz. Figure 9 gives measurement plot for the readout frequency equal to 1, 10, 20 and 30 MHz, respectively from left to right and top to bottom.
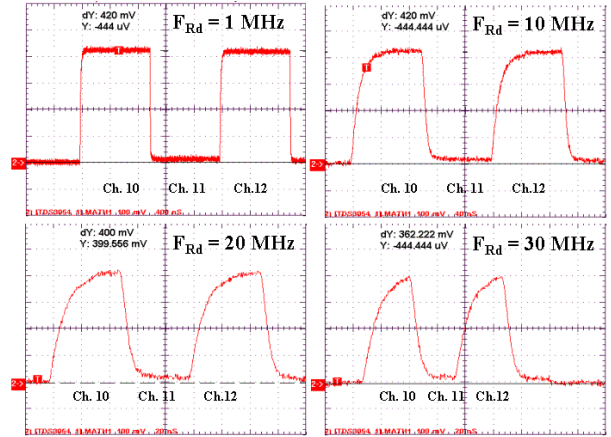

Fig. 9 Readout frames

10 MIPs signals have been injected to channels number 10 and 12. It can be seen that at a readout frequency of 20 MHz, the amplitude is almost the same as the amplitude for readout at 1 MHz. 20 MHz can be considered as the maximum readout frequency.

E. High input rate requirement

In the Inner Tracker System (ITS) of the ALICE experiment, the maximum occupancy is stated as 4% in Pb-Pb collision. It has been estimated that an average rate per channel is 100 Hz. In this case HAL25 chip will not present any pile-up phenomenon. However with new requirement of higher input rate, pile-up will occur in the circuit. The pile-up depends on the input signal time intervals, the input signal amplitude and the decay times both in the preamplifier and in the shaper. [3]

The decay time in the preamplifier is in the range of a few milliseconds corresponding to a few hundred of Hz. Reducing the value of the feedback resistor Rf in the preamplifier can reduce its decay time. This is done by decreasing the bias value VPRE (Fig. 10). In this case we have to accept some degradation in terms of noise and gain. The reduction limit of the decay time in the preamplifier is the decay time in the shaper, which is 8 times of the peaking time corresponding to a few tens of KHz.
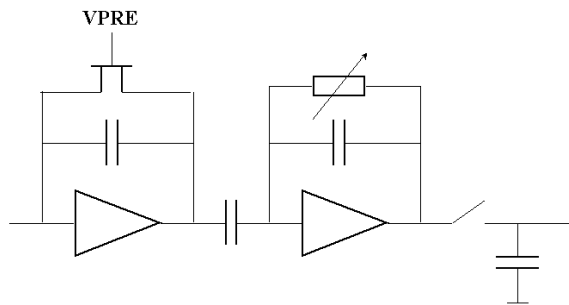

Fig. 10 Schematic of the front-end amplifier

F. Irradiation Test

HAL25 has been irradiated by an X-ray source up to 500 Krad that is much higher than the maximum irradiation dose expected than in the SSD of the ALICE experiment. No degradation was observed.

HAL25 Yield

The yield has not increased in the second version of HAL25. Around 50 % circuits have good performances that meet the specifications among the 340 tested circuits. The tested wafers have the same pattern of the wafer map. That means, the good circuits are located at periphery of wafers, while moving toward the center, circuits have too high power consumption.

Big efforts have been made to understand the yield problem in Strasbourg. We did thermal analysis with crystal liquid to locate failure points. We made passivation opening of circuit in order to micro probe areas in where we guess to have problem. We also took advises from CERN who reports to the foundry.

Although the Design Rule Checkers (DRC) do no detect any antenna error, chip failures seem to relate to long metal lines like for example, common biases and slow control lines in 128 parallel structures. May be the verification tools used for this deep submicon process are not well tuned for these analogue design practices which are usual in our community.

A new version has just been submitted in September 2002 in order to understand yield issues. In parallel, test structures have been implemented on the same wafer by CERN for the same purpose.

Conclusion

A new mixed ASIC intended for read out of SSD in the ALICE tracker has been designed in a deep submicron process. The correct functionality of the chip has been verified.

The third version circuit HAL25_V3 has just been submitted. The main objective of the submission is still to improve the yield. We also implement the new ESD protection of the I/O pads, low power LVDS Rx pads and a fuse programmable chip serial number unit.

Further evaluation of HAL25 will be performed after different steps: micro-cable bonding (TAB) of a bare chip, then a hybrid of six chips and detector.

References

[1] G. Anelli 'Conception et Caractérisation de Circuits Intégrés Résistants aux Radiations pour les Détecteurs de Particules du LHC en Technologie CMOS Submicroniques Profondes', Ph.D. thesis, INPG, December, 2000.

[2] C. Hu-Guo et al. 'The HAL25 Front-End Chip for the ALICE Silicon Strip Detectors' Proceeding of the 7th Workshop on the Electronics for LHC Experiments, Stockholm, Sweden, September 2001.

[3] C. Hu-Guo, C. Colledani, J.D. Berst 'Pile-up phenomena in HAL25', ftp://lepsi.in2p3.fr/pub/HAL25/Pile_up.pdf