

Development of the Inner Tracker Detector Electronics for LHCb

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Abstract

For the LHCb Inner Tracker, 320 μm thick silicon strip sensors have been chosen as baseline technology. To save readout channels, strip pitch was chosen to be as large as possible while keeping a moderate spatial resolution. Additional major design criteria were fast shaping time of the readout frontend and a low radiation length of the complete detector.

This paper describes the development and testing of the Inner Tracker detector modules including the silicon sensors and the electronic readout hybrid with the BEETLE frontend chip. Testbeam measurements on the sensor performance including signal-to-noise and efficiency are discussed. We also present performance studies on the digital optical transmission line.

I. INTRODUCTION

LHCb is a dedicated experiment at the future LHC collider for studying CP-violation in the b-quark sector. It has been designed as a single-arm forward spectrometer with a dipole magnet and an acceptance angle of 300 mrad in the bending plane. Due to the expected large number of tracks, the detector tracking system has been divided in an Outer Tracker based on straw tubes and an Inner Tracker, covering the high occupancy area around the beam pipe. Further detector components are the vertex detector (VELO) for exact determination of the position of secondary vertices, two separate RICH detectors for particle identification as well as an electronic and hadronic calorimeter together with a muon tracking system.

II. DESIGN OF THE INNER TRACKING DETECTOR

The baseline technology for the Inner Tracker was chosen to be 320 μm silicon strip detectors [1][2]. As the momentum resolution will be dominated by multiple scattering of the particles, a modest tracking resolution of 70 μm is sufficient. In order to minimise the number of readout channels, the strip pitch of the sensors has been chosen to be 198 μm . Multiple scattering is reduced by a small radiation length of the complete detector. As the detector will be located directly around the beam pipe, the frontend electronics have to

withstand the high expected total ionizing doses and particle fluences during the planned 10 years of lifetime of the experiment.

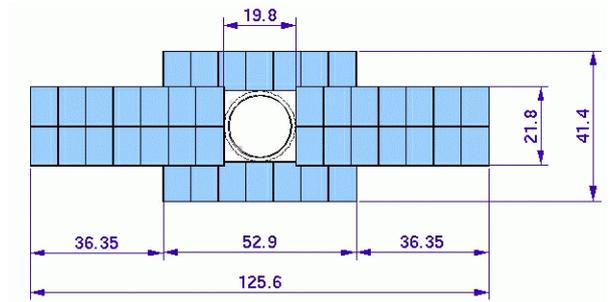


Figure 1: Layout of a single Inner Tracker station layer.

A. Sensor ladder and readout hybrid

The silicon strip detectors are made from a 6'' p⁺n wafer, and have an approximate size of 110 mm x 78 mm with 384 strips at a pitch of 198 μm . For covering the complete area of the Inner Tracker, a ladder design has been chosen with a maximum number of two sensors with their strips connected in series.

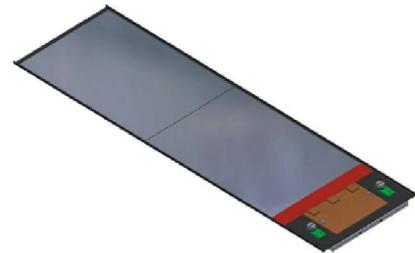


Figure 2: Silicon detector ladder with readout hybrid [3].

The ladder itself is made out of a heat conductive fiber composite to keep the temperature of the silicon sensors below 5°C. This reduces the leakage current of the detectors and in consequence the shot noise of the sensors after Irradiation. Interfaced by a pitch adapter made out of alumina, the frontend hybrid will be connected to the silicon sensors. Produced of 4-layer polyimide, it carries three BEETLE readout chips [4]. One chip can sample 128 channels and store the data in an analog pipeline. When triggered the analog data of the 128 channels are multiplexed on four differential analog outputs, therefore ensuring a total readout time of under 1 μs .

Any further use of amplifying circuitry close to the detector is prohibited due to the high radiation doses at the location of the readout hybrid, which is in the order of 1 Mrad over a projected lifetime of 10 years. The only solution for this is to route the analog signals to a so called ‘service box’ located on the Outer Tracker frame, where less radiation is expected.

B. Service Box

Further processing of the analog data is done in the service box, which is placed separate from the detector box.

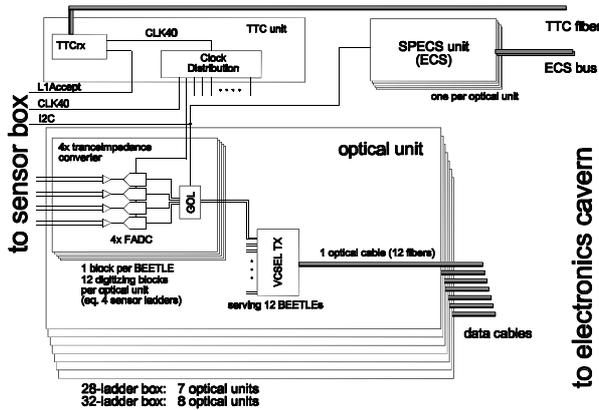


Figure 3: Block diagram of service box [5].

Outside the detector acceptance, the constraints on the material budget and the power dissipation are significantly lower. In a first step, the differential current signals have to be converted into a voltage signal, which are digitized by an AD9042 FADC [6]. This FADC has a 12 bit resolution and has been chosen because CMS ECAL has already done radiation qualification for it [7]. Still, the power dissipation is rather high and combined with only one channel per chip, the overall efficiency of this device is quite poor for our needs. Alternative FADC options are still under investigation.

The most significant 8 bits of the digitized data are connected to the CERN GOL serializer [8], which can handle 32 bits at 40 MHz in the fast mode operation. At the present design stage, we are using the current mode logic (CML) line driver, although a second driver capable of directly interfacing to plain VCSEL diodes is implemented in this chip.

One initial problem of the GOL serializer is the clock jitter requirement, which at the moment is lower than the clock jitter that can be delivered by the TTC system [9]. Although non rad-hard solutions are available [5], CERN microelectronics is working on a solution of this item.

The CML signals of 12 GOL chips are connected to a parallel optical transmitter with 12 VCSEL diodes. The transmitter directly interfaces to a commercial MTP fiber cable interface.

Taking into account the high power dissipation of the FADC chips, the current power estimate of the service box sums up to approximately 250 W. This, however, does not include the low voltage regulators for the frontend hybrid power supply, which are also located in the service box. Adding another estimated 300 W, the total power dissipation of this service box would be in the order of 550 – 600 W, which implies the need for an active cooling. Standard solutions can be employed because of the location outside the acceptance of the detector.

C. Optical Readout Link

Readout links based on direct electrical connections suffer from various disadvantages such as electromagnetic interference (EMI) including crosstalk, pickup and ground loops, loss of signal integrity over long cable lengths and little possibilities of data compression. With the development and commercialization of highly integrated optical components, the traditional drawbacks of optical transmission like higher complexity and price become smaller.

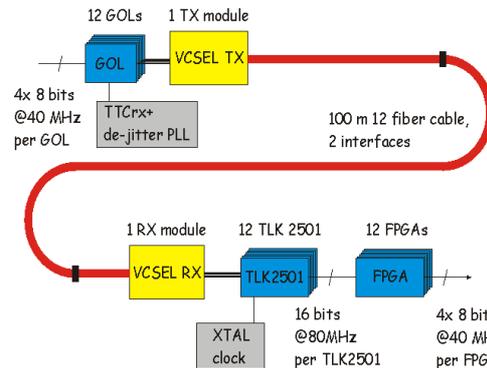


Figure 4: block diagram of digital optical readout link.

For the Inner Tracker readout design, a digital parallel optical system was chosen. The decision to run the transmission line digital was mainly driven by the argument of signal integrity in conjunction with the very good availability of commercial digital optical components. In the last years, several companies like Agilent Technologies [10] or Infineon Technologies [11] have started developments of a 12 fiber parallel optical link design, which lead to several multi-source agreements [12] [13] and common interfaces such as the MTP optical interface or the CML electrical interface for these devices. This resulted in a large number of companies capable of producing such modules, which in consequence leads to the assumption of a possible standard for parallel optical interconnects.

The transmitter module interfaces to a 12 fiber ribbon cable with a MTP connector. This optical interface has been used for over a year now at a system at the H1 experiment at HERA without any problems [14].

Table 1: Calculated optical power budget.

	typical	worst case
launch power	- 8 dBm	- 5 dBm
98 m multimode fiber	- 0.4 dB	- 0.3 dB
4 MTP interfaces	- 2.0 dB	- 1.2 dB
power after fiber	- 10.4 dBm	- 6.5 dBm
receiver sensitivity	- 15 dBm	- 18 dBm
power margin	4.6 dB	11.5 dB

The calculated optical power budget for the link is shown in Table 1, under the assumption of typical and worst case values for the connection and fiber losses. The result is a guaranteed power margin of more than 4 dB, with a typical power margin of more than 11 dB. The bandwidth of the fiber is 160 MHz-km, resulting in a bandwidth of 1600 MHz for a length of 100 m. This is well beyond the bandwidth of 800 MHz used by a 1.6 Gbit/s transmission.

The receiving side consists of an optical receiver closely resembling the transmitter, which converts the 12 optical signals in electrical CML level signals.

D. Demultiplexing and L1 Readout Board

To demultiplex the CML data stream, a commercial TLK2501 device from Texas Instruments [15] is used. The chip interfaces directly to one differential CML signal, deserializing it to 16 bits with a clock speed of 80 MHz (twice the GOL clock). In a first design, the second stage demultiplexing from 16 bits to 32 bits is done by a small FPGA [16] for making the complete readout link transparent: one digital input matches to one digital link output. For the final design, this demultiplexing stage might be implemented in the FPGA of the L1 readout board, which is based on the L1 readout board of the LHCb VELO vertex detector [17]. Current ongoing efforts in the LHCb group to unify the design of the L1 readout board for the VELO, Inner Tracker, Outer Tracker and RICH might lead to a common board design with different FPGA programming and mezzanine boards interfacing to the different readout links of the subdetectors.

III. STATUS OF HARDWARE

A. Sensor Ladder

The first full size sensor ladders have been taking data in May 2002 at the CERN X7 testbeam [18]. A 1-sensor ladder and a 2-sensor ladder were read out by a prototype polyimide hybrid with 3 BEETLE 1.1 frontend chips each. The data was transmitted and digitized with a HERA-B VDS readout system. Multi-geometry sensors were used to study the effects of different ratios of strip width to strip pitch. The differences in interstrip charge loss of a 200 μm and a 240 μm pitch sensor region were also investigated.

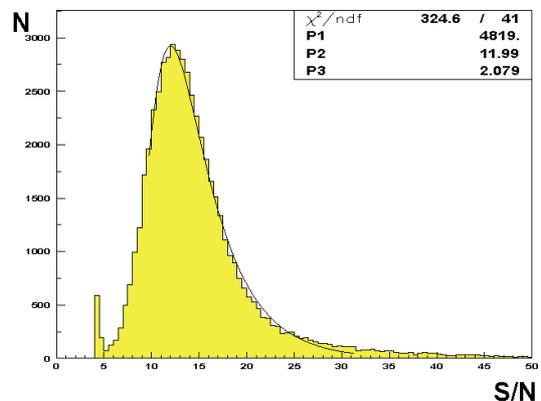


Figure 5: MIP signal S/N plot with the 22 cm long ladder.

Preliminary results from the data analysis show a signal to noise ratio of 11 for strip lengths of 22 cm (Fig. 5). Also observed has been an interstrip efficiency in the order of 96 % only (Fig. 6). However, this efficiency loss disappears with a slightly longer shaping time of the BEETLE preamplifier. The measured resolution of the sensors was better than 60 μm , well within expectations for the size of the strip pitch and the requirements of LHCb (Fig. 7).

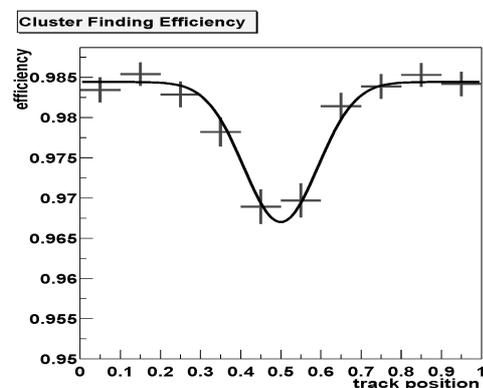


Figure 6: Efficiency vs. inter-strip position.

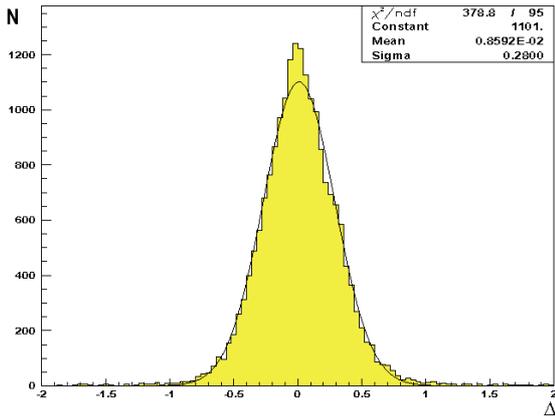


Figure 7: Resolution of 200 μm pitch sensor.

B. Optical Readout Link

First light of the readout link was established during Summer 2002. For this, a BEETLE 1.1 baseline was digitized by a non rad-hard 8 bit FADC [19] running at 40 MHz. The resulting digital data were multiplexed by a GOL 0.1 chip. PR2000 optical modules from Paracer Inc. were used to send the data over 98 m of optical cable¹, including 2 optical cable interfaces to simulate a possible LHCb installation. For demultiplexing, a printed circuit board with the TLK2501, a low-jitter crystal oscillator and a FPGA was developed. Together with the GOL multiplexer, this circuit provided a fully transparent link and therefore easy debugging and evaluation of the functionality. Analysis of function was simplified by connecting the transmitted 8 bits to a DAC [20] also running at 40 MHz. The reconstructed analog baseline could easily be verified and checked against the original generated signal on a scope.

A TTCvm unit serving as an optical clock source was used to generate a 40 MHz master clock. A TTCrm mezzanine card equipped with a TTCrx 3.1 decoded the optical signal and generated a 40 MHz clock. However, this has been found to have a peak-to-peak jitter of approx. 150 ps, which is well above the clock input specification of the GOL serializer of 100 ps. Therefore, an external low phase noise PLL was built to clean up the clock signal. The resulting peak-to-peak jitter was below 80 ps and was considered to be sufficient for low bit error GOL operation.

Operation of the readout link is perfectly stable over a period of 9 hours with no observable errors. However, a proper bit error rate test has not yet been done, but is planned by the end of this year.

C. L1 Readout Board

The current RB2 prototype board is in use by the VELO group and has been verified to work together with the BEETLE 1.1 in a testbeam period in October 2001. The RB3 successor is currently under construction at the University of

Lausanne. Further integration work with the Inner Tracker electronics is planned.

IV. RADIATION

When considering radiation effects, we can limit our discussion to the Inner Tracker system from the silicon sensor up to the first couple of meters of the optical fiber, as radiation levels drop significantly outside the detector. For the detector box holding the sensor ladders, a maximum radiation dose of 1 Mrad together with 10^{13} n/cm² of neutron fluence are expected [21]. While the BEETLE 1.1 has been irradiated up to 45 Mrad without showing any damage [22], the silicon sensors were not yet irradiated. However, the expected radiation damage is likely to be under control with cooling down the sensors to below 5°C for keeping the leakage current low and in consequence the shot noise of the detector small.

When moving further away from the detector box to the service box, the total ionizing dose drops to a level around 10 krad with a neutron fluence of around 10^{12} n/cm². As already stated, the FADC has been radiation qualified. However, the optical transmitter module has an unknown radiation tolerance and is likely to be SEU sensitive because of an internal factory programmed flash memory for the bias settings of the VCSEL laser drivers. A backup solution is using a similar optical package with a commercially available 12 VCSEL diode array only and the internal GOL laser driving circuitry. A third option would be to use 12 VCSEL diodes with single fiber interfaces and a so called breakout cable for joining 12 single fibers to the 12 fiber ribbon cable. This is most likely to be rad-hard, because of the high radiation tolerance of the VCSEL diodes, which have been qualified before [23]. All three options are under investigation and will be prepared for a planned irradiation test in Spring 2003.

Effects on the fiber are limited to radiation induced attenuation. CMS has irradiated fibers and presented the results in [24]. The highest measured attenuation measured was in the order of 0.1 dB/m at a dose of 1 Mrad. Neutron induced attenuation was found to be in the same order for fluences of $4 \cdot 10^{13}$ n/cm². When taking into account the significantly lower radiation levels in our environment, the expected attenuation should be below 1 dB for 10 m of fiber. However, this is also planned to be measured in the irradiation test.

¹ Produced by Opticonx Inc.

Table 2: Cost estimate for optical readout system.

Component	Component cost	needed per analog Beetle output	cost per analog link (CHF)
FADC AD9042	USD 31.20 = CHF 50	1	50.00
GOL serializer	CHF 20	1/4	5.00
optical transmitter	USD 530 = CHF 780	1/48	16.25
optical ribbon	USD 600 = CHF 930	1/48	19.38
optical receiver	USD 530 = CHF 780	1/48	16.25
TLK2501 deserializer	USD 21.60 = CHF 34	1/4	8.50
16:32 bit demultiplexer	USD 8.80 = CHF 14	1/4	3.50
80 MHz XTAL (low jitter)	CHF 6.60	1/4	1.65
	1USD = 1.60 CHF		120.53

V. COST ESTIMATE

A cost estimate of the digital optical readout link is shown in Table 2. For comparing this to a plain analog readout design, the costs have been scaled down according to the transmission capability of the device under discussion. Quoted are prices for volumes needed for a full Inner Tracker readout. As the FADC is contributing with more than 30 % to the overall system cost, cheaper options are currently under review. One alternative would be the MAX1195 ADC with a price well below 10 CHF. However, this device has yet to be qualified for the radiation levels expected at the location of the service box .

VI. CONCLUSION

A full size prototype of a 2 sensor silicon strip sensor ladder has been developed and data were taken with the BEETLE 1.1 running at 40 MHz. Signal-to-Noise values of 11 were achieved with sensor strip lengths of 22 cm. This is expected to improve with the new BEETLE version 1.2, which is at the moment undergoing first tests. The first prototype of a multi-layer polyimide frontend hybrid proved to work. A digital optical readout system has been designed and set up as a prototype. Stable operation with a layout comparable to LHCb requirements has been verified together with a first set of TTC system components. A cost estimate for a complete LHCb readout showed a price comparable to conventional copper readout designs. Several system components already have been qualified for the expected radiation doses and particle fluences expected during the operational period of LHCb. Those components not tested yet are scheduled to be tested in Spring 2003. Backup solutions in case of radiation sensitivity have been presented for several parts.

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