

# System Performance of ATLAS SCT Detector Modules.

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## *Abstract*

The ATLAS Semiconductor Tracker (SCT) will be an assembly of silicon microstrip detector modules on a large scale, comprising 2112 barrel modules mounted onto four concentric barrels of length 1.6m and up to 1m diameter, and 1976 endcap modules supported by a series of 9 wheels at each end of the barrel region. To validate the electrical performance a "system test" has been established at CERN.

This paper gives a brief overview of the SCT, highlighting the electrical performance of assemblies of modules studied at the system test. The off detector electronics and software used throughout these studies is described.

## I. INTRODUCTION

An SCT module comprises two planes of silicon microstrip detectors glued back to back. Small angle stereo geometry is used to provide positional information in two dimensions, an angle of 40 mrad being engineered between the axes of the two sides. The barrel module uses two pairs of rectangular detectors with parallel strips to give an active strip length of approximately 12cm. Three designs of different radial geometries are used in the endcap region: inner, middle and outer modules.

A module is read out by 12 ABCD3TA ASICs [1] mounted on a copper/kapton hybrid. Manufactured in the radiation hard DMILL process [2], each chip provides sparsified binary readout of 128 detector channels. The amplified and shaped input signal is compared to a programmable threshold having two components: a single 8-bit DAC applied across the whole chip, and a channel specific 4-bit DAC designed to compensate for channel-to-channel variations. The resulting hit pattern is transferred into a binary pipeline, 132 cells deep. Upon receipt of a Level 1 Accept (L1A) trigger, the pipeline output is transferred into a derandomising buffer that can store up to 8 events.

The clock and command signals are transmitted to the module in the form of a biphasic mark encoded optical signal. In turn the off detector electronics receives two optical data streams back from each module. The DORIC and VDC ASICs are used in the conversion of these signals between optical and electrical form at the module end [3].

The first chip on each side of the module, designated as the master chip, is responsible for the electrical transmission of data to VDC. Within the module a token passing scheme is used to control the transfer of data to the master chip for

onward transmission. This scheme incorporates several redundancy options such that, should any single chip fail, the remaining chips can still be read out.

Each SCT module is connected to its own programmable low voltage and high voltage power supply channels. The power distribution system includes three patch panels and three lengths of conventional cable, the innermost section being formed by low mass power tapes to minimise the material in the tracker volume. In the endcap module the power tapes connect directly to the hybrid, upon which the opto communication ASICs are mounted. The associated pin diode, VCSEL laser diodes and their coupled fibres are housed on a small plug in board. In the barrel region the interface between the module, power tapes and optical signals is provided by a further copper/kapton flex circuit. Each module initially dissipates around 5.5W, with a maximum of 10W allowed for after irradiation: the removal of heat is an important aspect of the module and system design.

The binary architecture of the SCT dictates that great attention must be paid to the system design since an excess of common mode noise could render the detector blind. There are significant stray capacitances between modules and system components that have been considered during the development of our grounding and shielding proposals. To understand the performance of the system, analogue information may be extracted by scanning chip thresholds.

The system test was set up to study the performance of the SCT system, to refine the grounding and shielding design and to demonstrate its resilience against external noise sources. This paper documents some of the techniques that have been developed for these studies, and some of the results that have been recorded.

## II. READOUT SYSTEM

Although the system test is being used as a proving ground for the final ATLAS SCT off detector electronics and power supplies as they become available, the majority of studies to date have been performed using a set of custom VME modules. A schematic diagram of the readout system is shown in Figure 2.

The CLOAC MASTER module provides the system wide 40.08MHz clock and generates fast commands such as L1A. Fast commands may be generated in response to external trigger sources although most commonly at the system test individual triggers are generated in response to VME commands. The CLOAC FANOUT module generates

multiple copies of the clock and fast command signals for distribution to other modules.

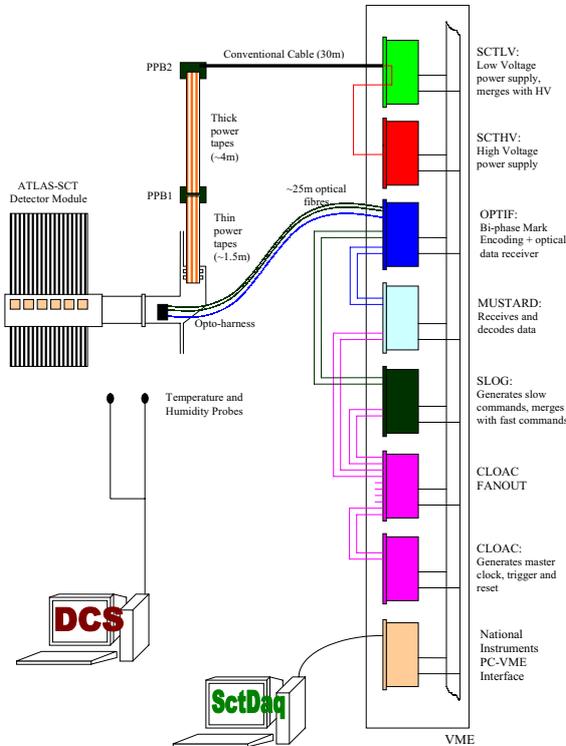


Figure 1: Schematic diagram of Barrel Readout System

SLOG distributes the clock and fast command signals generated by CLOAC to up to 12 detector modules. It also generates the slow command data needed to configure the detector modules. MuSTARD receives data from up to 6 detector modules, or 12 data streams, decoding the events and histogramming the data. Individual events may be transferred to the host computer if more detailed analysis is required.

OptIF provides the interface between the optical and electrical domains for six detector modules, matching the modularity of MuSTARD. Discrete VCSEL lasers transmit the biphase mark encoded clock/command signal, generated by BPM4 chips, to the modules. Packaged arrays of pin diodes are used to receive the returned data.

Each SCTLV module provides low voltage power for two detector modules and their associated optical components. Three generations have been used, the most recent of which adds readout for the NTC thermistors mounted upon the SCT modules. The companion module SCTHV provides detector bias at up to 500V for four detector modules.

The VME crate is interfaced to a PC running Windows NT or more recently, Linux, by means of National Instruments' PC-MXI-2-VME interface set. SCT module configuration and data acquisition is performed by the SCTDAQ software

package [4]. Static libraries written in C handle the basic communication with the VME boards. Higher level functions are implemented in a small number of C++ classes, linked with the static libraries and some libraries of the ROOT framework [5], to form a shared library.

Within ROOT, the system is started by running an interpreted macro that calls upon the functions of the shared library to initialise the VME boards and configure the SCT detector modules to their default operating conditions. Simple tests and configuration changes may be performed directly from the CINT console; more complex tests have been implemented in the form of additional interpreted macros.

### III. TEST PROCEDURES

Many test procedures and analyses have been developed for use with SCTDAQ, including those used for the characterisation of hybrids and modules during production [6]. The procedures most commonly used at the system test are outlined below.

#### A. Three Point Gain

Threshold scans are performed for injected charges of 1.5, 2.0 and 2.5fC. In each case a complementary error function is fitted to the data: the mean corresponds to the threshold at which 50% efficiency is achieved for pulses of the designated magnitude and the sigma is a measure of the output noise (in mV). The gain of each channel is calculated from a linear fit to the fit results for the three scans. The output noise from the scan taken with 2.0fC injected charge is divided by the gain to determine the input noise (in fC or ENC).

#### B. Single Threshold Scan

A single threshold scan is performed for an injected charge of 2.0fC. The input noise is estimated from the measured output noise and the known average gain of each chip, which has been shown to remain constant over periods of many hours. This is one of the fastest methods that can be used to make comparative noise measurements.

#### C. Noise Occupancy Scan

A threshold scan is performed without charge injection to determine the noise occupancy of each module as a function of threshold. Analysis of the data permits an estimation of the (Gaussian) noise of each module by means of a linear fit to a graph of  $\ln(\text{occupancy})$  vs  $Q_{\text{thr}}^2$  (fC<sup>2</sup>). Deviation from this line, notably at higher thresholds, is indicative of non-Gaussian behaviour such as the presence of common mode noise.

#### D. Repeated Noise Occupancy

Here the modules are configured to a fixed threshold and repeated measurements of noise occupancy are made to monitor the stability of the system. Events are recorded sequentially: each complete event must be processed by MuSTARD before the next L1A trigger is broadcast to the

modules. The threshold chosen for such studies is typically 1fC, the nominal operating threshold of the ATLAS SCT.

### E. Correlated Noise Studies

Data is acquired in the same manner as for a Noise Occupancy measurement, however each event is now written to a file. Analysis of the common mode component of the noise may be performed offline [7].

### F. Multiple L1A Studies

Two L1A triggers are sent to the module, separated by a specified number of clock periods. The first event of the pair is thrown away leaving the second event to be histogrammed. By varying the spacing of the two triggers the occupancy of the modules is determined at various points during the readout cycle. In ATLAS, events will be recorded as data transmission is taking place; it is important that any electrical activity correlated with data transmission does not feed back to the front end.

## IV. THE BARREL SYSTEM TEST

The Barrel System Test is based around a prototype sector built to support 48 modules. Four harnesses are mounted on the sector, three on the left hand side and one on the right hand side. Each harness provides electrical services for six modules. To date, up to 16 modules have been operated at any one time.

One configuration, consisting of twelve modules in a row, is shown in figure 2. The electrical services for the harnesses mounted to the left and right hand sides of the barrel leave the detector at opposite ends. In ATLAS, these cables will be routed to power supplies separated by a large physical distance. Any difference in potential between adjacent modules could be a source of common mode noise.

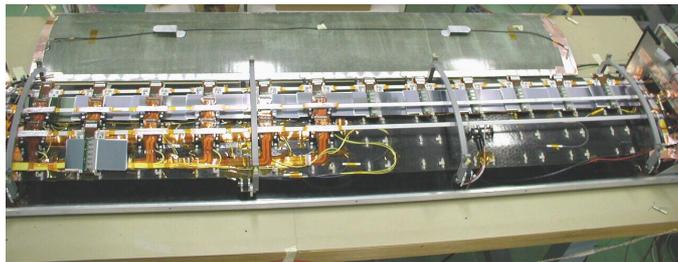


Figure 2: Twelve Modules in a row on the Barrel Sector

The grounding and shielding arrangement is described in the SCT/Pixel Grounding and Shielding notes [8] and [9]. Certain connections have been implemented in a reversible way to facilitate the study of variations upon the basic scheme.

Each barrel module is built around a baseboard designed to have good thermal performance, moving the heat towards the cooled area [10]. At its core is a sheet of VHCPG (Very High thermal Conductivity Pyrolytic Graphite), an electrically conductive material. Although electrically insulated by a beryllia sheet, there remains capacitance between the VHCPG

sheet and the cooling block of approximately 100pF. Since the VHCPG also forms part of the bias circuit for the silicon microstrip detectors, this is a route by which unwanted signals may reach the front end.

Two options have been considered as a means of controlling this signal path. The default solution uses a “shunt shield”, a sheet of kapton-backed copper connected to the module ground reference and placed between the module baseboard and the cooling block. With the shunt shield in place, any variation in the potential of the cooling pipe will induce current on the shield rather than the module baseboard, hence the resulting signal is shunted to the module ground. To further control any currents that may flow through the cooling pipe, each one is split into two electrically isolated halves to match the routing of the electrical services. Each half pipe is connected to its respective end plate.

The alternate solution makes a DC connection between the cooling pipe and the module ground reference such that the potential difference between the two is minimised. In parallel with this the cooling pipe is no longer split into two halves. At the system test this scheme is implemented by making an electrical connection between the two halves of each cooling pipe and by shorting each shunt shield to the cooling circuit.

Both solutions perform equally well in the absence of noise injection. The noise of each of a group of 12 modules mounted on the sector, measured by the Three Point Gain method, is shown in figure 3. The data is displayed to match the physical arrangement of the modules as shown in figure 2; for example, module 0035 was mounted in the far left position. Each marker represents the mean noise observed in one chip: within a module the first chip is on the top face at the edge nearest the cooling contact with the last chip located almost directly underneath.

The figure also shows reference data taken using electrical readout before each module was mounted on the sector: many modules perform slightly better on the sector than they do in an aluminium test box.

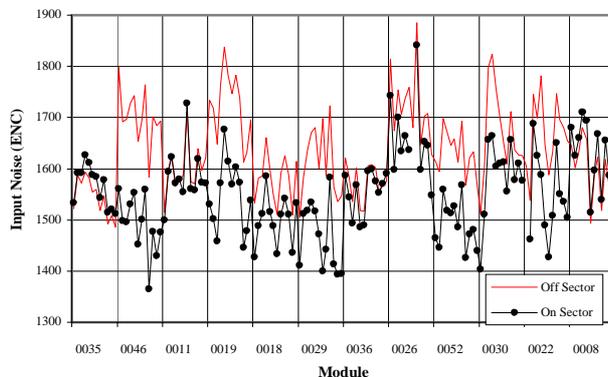


Figure 3: Comparison of Noise measured Off and On the Sector

The noise occupancy of the modules at the nominal operating threshold, 1fC, is shown in figure 4. The occupancy of each module is significantly below the design target of  $5 \times 10^{-4}$ .

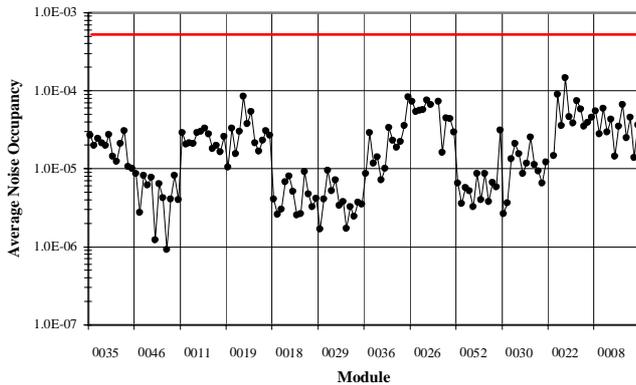


Figure 4: Average Noise Occupancy at 1fc Threshold

In order to probe the detailed performance of each grounding and shielding configuration, noise is deliberately injected into one or more components of the system. Early studies showed the system to be most susceptible to pickup at frequencies of order 10MHz, in agreement with the bandpass characteristic of the front-end amplifier.

The set up used to inject noise into the barrel shield is shown in figure 5. The output of a signal generator is coupled to a large, rectangular ferrite. A wire is passed through the ferrite, connecting to the “heat spreader plate” at each end of the barrel shield near its union with patch panel PPB1. Noise may also be injected directly into the power supply chain by placing the ferrite around one or more conventional cables or bundled power tapes.

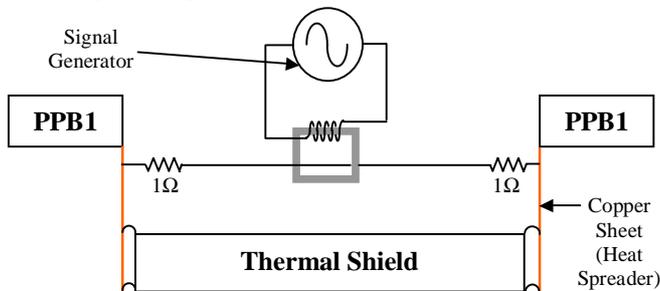


Figure 5: Injection of Noise into the Detector Shield

The single threshold scan method is used to observe the effect that the injected noise has upon the detector. In each configuration a reference scan is recorded with the signal generator amplitude set to zero. The amplitude is then increased and the scan repeated. Analysis of the two scans yields a measurement of the excess noise on each chip.

An example of such a study is shown in figure 6. A large signal was injected into the shield to provoke a response from the system. The signal generator was set to produce a 10MHz sine wave of 10V amplitude. Each marker represents the excess noise observed on one chip. Although other configurations were studied, the results are shown only for the two basic schemes: default (squares) and alternate (circles). The chips most affected are typically those furthest away from the module cooling contact, however the performance of the alternate configuration was found to be better than the default scheme.

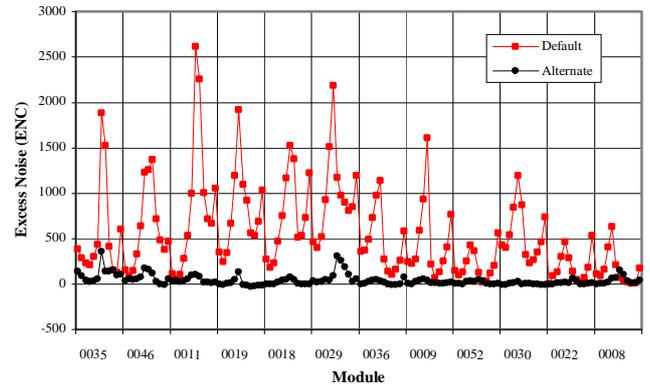


Figure 6: Excess Noise with Noise Injection into the Shield

Similar work has been performed injecting noise into the bundle of low mass tapes serving the harness mounted on the right hand side of the sector, and into the conventional cable providing electrical services to one of the modules. In both cases there was less to choose between the performance of the two schemes, although the default scheme was more robust against noise injected into the conventional cables.

Both the default and alternate configurations remain as options for use in the final ATLAS SCT. The decision between them will be made after noise injection studies have been repeated using a full set of pre-series production components. Meanwhile studies continue to examine the resilience of the present system test shield against injected noise of different frequencies, and to determine the common mode component of the observed noise.

## V. THE FORWARD SYSTEM TEST

The Forward (End-Cap) System Test is based around a carbon fibre sector, equivalent to one quarter of a disk. This is mounted on an aluminium support frame within a copper enclosure representative of the thermal shield. A total of 13 outer modules and 10 inner modules may be mounted on the front of the sector and 10 middle modules on the back. A close up showing four outer modules mounted on the sector is shown in figure 7.

A total of 33 designs of “wiggly” low mass tape are required to service a full quadrant. For the system test, 9 designs have been produced which were fitted to the disk as best as was possible. Opto-harnesses comprising optical fibres and plug-in PCBs are used to provide clock and control signals for groups of 5 or 6 modules.

The grounding and shielding scheme used in the forward system test is again based upon that described in references [8] and [9]. All cooling blocks are electrically tied to the surface of the disk, and to the shield, through a system of foils applied to the disk’s surface.

Two shunt shields were integrated into the design of the K5 forward module. In the case of an outer or middle module, there exists approximately 50pF capacitance between the electrically and thermally conductive module spine made of TPG (Thermal Pyrolytic Graphite) and its two cooling

contacts. The first shunt shield ensures that noise developed on the module spine, due to changes in the potential of the cooling circuit, is shunted to the module ground reference. This is present in all configurations.

The second shunt shield protects the small signal ground from changes in the potential of the hybrid cooling block. This may be shorted out to give a DC connection between the module ground reference and the hybrid cooling block: at the system test this is accomplished by means of a copper braid placed between the cooling block and the module power connector. The latter configuration has been studied with and without a secondary tie between each module's digital ground line and the shield, made at patch panel PPF0.



Figure 7: Four Outer Modules on the Forward Sector

Noise levels at the forward system test were found to decrease with time. The time constants involved vary from module to module and can be as long as one hour. Similar behaviour has been observed in barrel modules, although in general the time constants are shorter. The underlying cause of the problem has been understood as an intrinsic time dependence of the detector interstrip capacitance [11]. For this reason the detectors are kept biased for at least one hour before any comparative noise measurements are made.

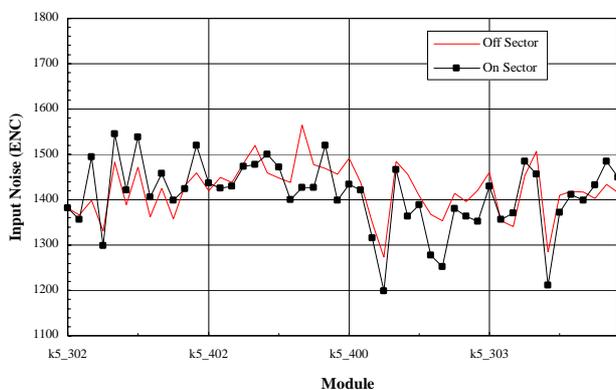


Figure 8: Noise of four Outer Modules, measured Off and On the Sector

Initial studies have shown good performance in the absence of noise injection. The noise measured for each of a group of four outer modules is shown in figure 8. The values have been normalised to the ATLAS operating temperature of 2°C. The noise occupancy of a group of four outer modules mounted on the sector is shown in figure 9. The occupancy of each chip is well below the limit of  $5 \times 10^{-4}$  imposed by the specifications.

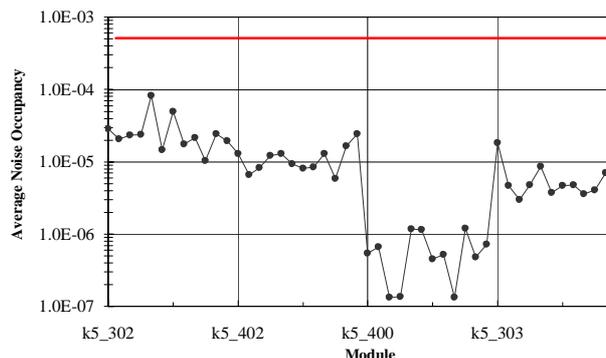


Figure 9: Noise Occupancy of four Outer Modules at 1fc Threshold

Studies of grounding and shielding are ongoing to minimise the susceptibility of the system to common mode noise.

## VI. SUMMARY

A system test of the ATLAS SCT has been established at CERN [12]. An extensive set of tools has been developed to probe the performance of the system. These tools have facilitated studies of several grounding and shielding configurations. The studies will continue using pre-series production components.

## VII. REFERENCES

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