The ATLAS Pixel Front End Chip FEI in 0.25µm Technology

P. Fischer for the ATLAS Pixel Collaboration

Physikalisches Institut, Bonn University, Nußallee 12, 53115 Bonn, Germany
fischerp@physik.uni-bonn.de

Abstract

The most recent front end chip FEI for the ATLAS pixel detector has been implemented in a quarter micron technology. Special layout rules have been used to enhance its radiation tolerance. The architecture and some implementation details of the FEI chip are presented.

I. Introduction

The ATLAS pixel detector will consist of 2-3 barrel layers and 2x3 disks in the forward and backward regions. The main elementary building blocks are pixel modules which are mounted on staves in the barrels and on sectors for the disks. The 13 modules on the staves (Figure 1) are shingled so that all particles hit at least one module in its active area (which does not extend all the way to the edge due to guard rings on the sensors). The individual staves in the barrel are tilted in a turbine-wheel fashion to ensure overlap in the phi direction as well.

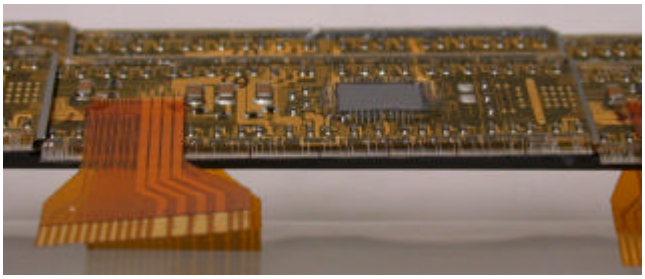

Figure 1: Prototype modules mounted on a stave. The modules are shingled to ensure that all particles produce at least one hit in the active area.

The sectors consist of two carbon-carbon faceplates onto which two/three modules are mounted from both sides ensuring, again, full coverage of the area. Both, staves and disks, are cooled to –6°C to reduce the effects of radiation induced damage in the silicon sensor. A high cooling capacity is achieved by evaporating a liquid in aluminium tubes running along the staves or between the faceplates for the disks.

A. The flex capton module

The central element of the module is a silicon sensor with n^+-type pixels in a n^--type bulk material [1]. Its active area in the center is subdivided into rectangular pixels of 50µm x 400µm size. 16 pixel readout chips are mounted below the sensor in two rows of eight chips. The electrical connection between the sensor pixels and the inputs of the individual pixel elements on the chip as well as the mechanical connection are achieved with 2880 bumps per chip. In order to avoid inefficient areas in the regions between two readout chips, the sensor pixels are 600 µm long in one gap and 2x4 extra pixels of 50 µm x 400/600 µm size are introduced in the other gap. These pixels are connected in parallel to other pixels on the sensor so that the information in that small area is ambiguous and must be resolved by pattern recognition.

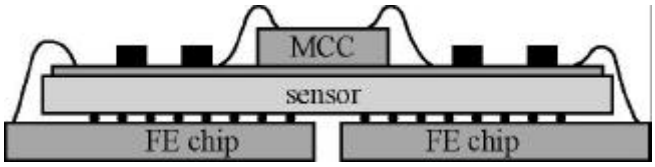

Figure 2: ATLAS pixel module. The front end chips are bump bonded to the silicon sensor in the active area. The IO part of the chips stands over the sensor so that a wire bond connection to a capton PCB glued onto the other side of the sensor can be made. The capton also accommodates passive components and a module controller chip (MCC).

A two layer capton PCB on top of the senor is used to supply power and control signals to the front end chips, to accommodate passive components (decoupling capacitors, termination resistors, temperature sensors) and an additional module controller chip (MCC) which collects the hit information from all 16 chips, builds events and sends the compressed data off the detector. The MCC also ensures the communication between the front end chips and the data acquisition. As indicated in Figure 2, the MCC is glued to the flex caption and connected with wire bonds. The front end chips are standing out over the sensor so that a wire bond connection to the flex capton can be made.

II. The FEI Chip

The geometry of the 7.4x11 mm^2 size chip is identical to the previous generations FEA/B/C (0.8µm CMOS) and FED (0.8µm DMILL, radiation tolerant). The 2880 pixels unit cells of 50 µm x 400 µm size are arranged in 18 columns x 160 rows. Every pixel cell contains a charge sensitive amplifier, a discriminator for zero suppression and a digital readout logic to transport the hit information to the periphery. The signal charge can be determined by measuring the width of the discriminator output signal. The hits are temporarily stored in the periphery in one of 64 buffers per column pair until a trigger signal selects them for readout. Hits with no trigger are discarded after the programmable trigger latency of up to 256 clock cycles of 25 ns (40 MHz bunch crossing clock of LHC). All hits belonging to one trigger are sent through one serial LVDS link to the module controller chip which builds full

module events containing the hit information of all 16 FE chips on a module.

The chip has been designed in a quarter micron technology with 5 metal layers using radiation tolerant layout rules [2]. Tests of the first batches received back from the vendor from January 2002 on showed that the design is fully functional. Assemblies of single chips with sensor and full modules have been operated since then successfully. Irradiations of chips to the full dose of 50Mrad expected after 10 years of LHC operation have shown no significant degradation of the chip performance.

The following sections describe the analogue part of the pixel, the readout concept and other interesting features of the design.

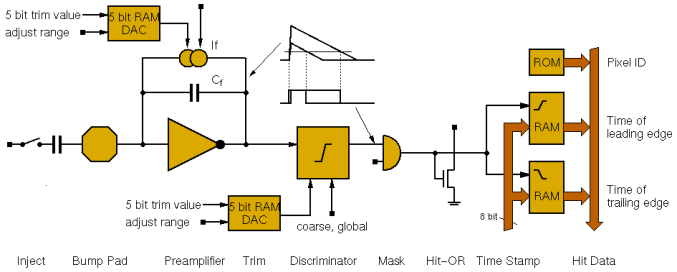

Figure 3: Block diagram of the pixel unit cell. The output signal of a charge sensitive amplifier is compared to a threshold voltage to detect individual hits. The time of the rising and of the falling edge of the discriminator output is recorded. Two 5 bits DACs per pixel are used to tune the threshold and the feedback current.

A. The Pixel Cell

Figure 3 shows a block diagram of the most important elements in the pixel cell. The charge deposited in the sensor is brought to the pixel through the bump bond pad which connects to the input of a charge sensitive amplifier. An inverting folded cascode amplifier is fed back by a capacitor of $C_f \sim 5fF$ integrated into the lower metal layers of the bump bond pad (a large value of 10 fF has also been implemented, but the larger gain of the smaller feedback capacitor is preferred). The feedback capacitor is discharged by a constant current so that the triangular pulse shape measured through a monitoring buffer in Figure 4 is observed. As a consequence of this particular pulse shape, the width of the discriminator output signal (the 'time over threshold', ToT) is nearly proportional to the deposited charge. The ToT is measured in FEI in units of the bunch crossing clock (25 ns) and provides an analogue information of every hit with a resolution of 4-6 bit. The feedback current I_f is set globally with an 8 bit on-chip bias DAC so that a compromise between a good ToT resolution (small I_f) and small dead time in the pixel (larger I_f) can be found. The feedback current can be fine-adjusted in every pixel by means of a 5 bit DAC for a possible time walk correction (see later). The constant feedback current generation is part of a circuit which compensates for detector leakage current. This must be sourced by the electronics because the pixel sensor is dc-coupled to the readout chip. The compensation circuit can cope with more than 100nA detector leakage current.

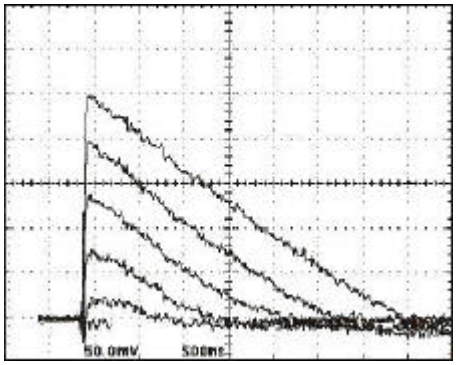

Figure 4: Output signal of the charge sensitive preamplifier for increasing input charges (approx. 5000-25000 electrons) measured through an on-chip monitoring buffer.

The 'coarse' threshold of all discriminators on the chip is set with an 8 bit bias DAC. A small threshold dispersion between the 2880 channels is crucial in order to achieve low threshold settings without an increased noise hit rate. The number of local trim bits in every pixel has therefore been increased to five. The range of these threshold tune DACs can be set globally so that a compromise between resolution and span can be found.

Every pixel contains a calibration circuit used to inject known charges into the input node. The circuit generates a voltage step (between a supply voltage and a global calibration voltage) which is connected to one of two injection capacitors. A 'low' range with a small capacitor is used for precise threshold scans while a 'high' range with a larger capacitor is available to study the behaviour for larger input charges.

The output signal of the discriminator in every pixel can be disabled with a local 'mask' bit. A fast 'OR' of a programmable subset of pixels is available for testing purposes and for a self-triggered operation of the chip (the OR signal is then delayed and used as a trigger).

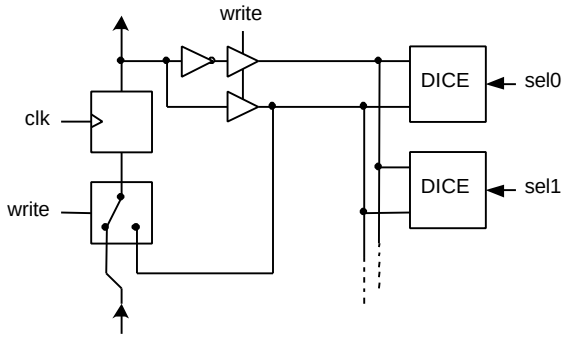

Figure 5: Control part in the pixel. A shift register is used to write the configuration information in one of 14 SEU tolerant DICE cells. The reading back of the bits is easily possible.

The basic philosophy of the readout is to associate the hit to a unique bunch crossing by recording a time stamp when the rising edge of the discriminator occurs. The time of the

falling edge is memorized as well so that the ToT can be calculated as the difference of the two values in units of the bunch crossing clock. The 2 x 8bit RAM cells used for this purpose are classical static memory cells. Only one hit can be recorded in the pixel so that the RAM values are transferred to buffers at the bottom of the pixel columns as fast as possible (see next section).

The 14 configuration bits used in every pixel (2 x 5 bit DACs, mask, enable_hitbus, kill_amplifier, inject_pixel) are stored in SEU tolerant DICE cells [3] which can be written and read back by means of a shift register running vertically through the column as illustrated in Figure 5.

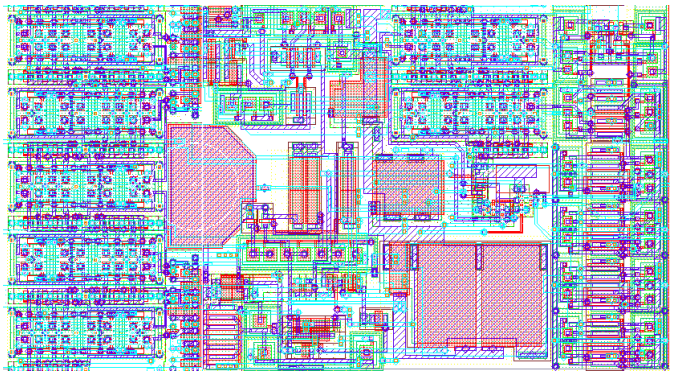

Figure 6: Layout of the analogue part + slow control of the pixel cell in FEI. This part is 50µm high and 90µm wide.

The layout of the analogue part of the pixel together with the slow control and the DICE cells is shown in Figure 6. The cell is 50µm high. On the left side, one can distinguish 10 DICE cells (22µm wide) and the two 5 bit DACs located above and below the bump pad. The slow control section and four more DICE cells are located on the right, amplifier, second stage, discriminator, leakage compensation and injection circuitry fill the central part.

B. *The Readout Concept*

The most important elements of the digital readout are sketched in Figure 7. Four elementary tasks are running in parallel:

1. Time stamps generated by an 8 bit Gray counter clocked with the 40 MHz bunch crossing signal of LHC are stored for the rising and the falling edge of the discriminators in the pixel. The pixel data is ready to be processed when the falling edge has occurred and a 'hit' flag in the pixel is set. The presence of at least one active hit flag in a column pair is flagged to the bottom of the column with a fast priority scan.

2. As soon as hits are flagged to the Column Control Logic, the uppermost hit pixel in the column is requested to send its rising and falling edge time stamp and its ID (hard coded address from a ROM in the pixel) down the column. This information is stored in a free location of the End-of-Column (EoC) buffer pool consisting of 64 locations per column pair. The pixel is then cleared and the scan continues the search for other hit pixels. Hits are thus transferred from the pixels to the EoC buffers at a programmable rate of 5-20 MHz.

3. The hits must stay in the EoC buffers until the trigger latency, i.e. the time difference between the hit occurring in the sensor and the arrival of the level1 trigger signal, has elapsed. The leading edge time stamps of the hits in the EoC buffers are therefore permanently compared to the actual time stamp minus the fix (programmable) latency. When the comparison is true and a trigger signal is present, the hit is flagged as 'valid for readout'. It is discarded (the EoC buffer location is freed) otherwise. The incoming triggers are counted on the chip. This trigger number is stored together with the 'valid for readout' flag in the EoC buffer so that several consecutive triggers do not lead to confusion. A list of pending triggers is kept in a FIFO.

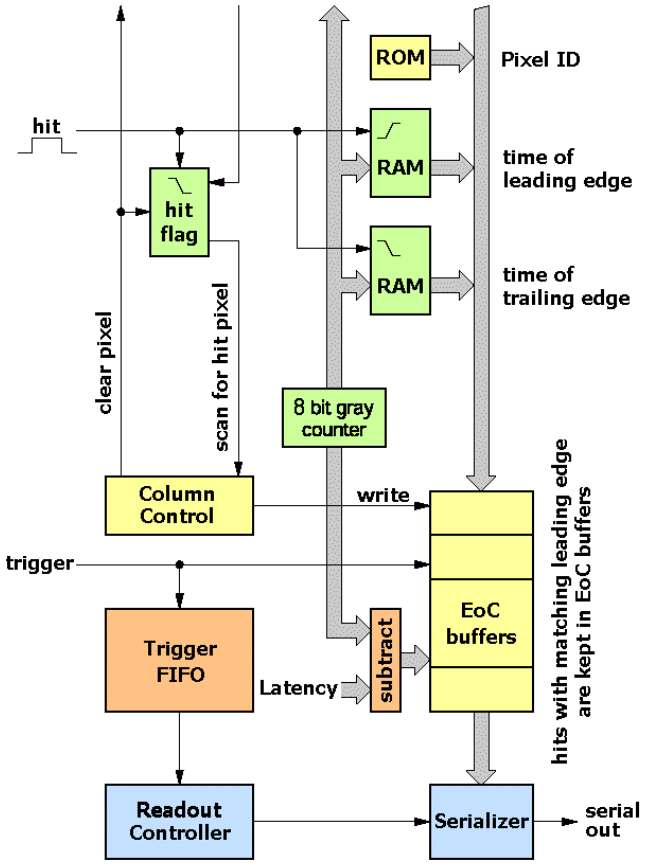

Figure 7: Important elements of the readout of FEI (see text).

4. A Readout Controller initiates the serial readout of the hit data as soon as pending triggers are present in the Trigger FIFO. The EoC buffers are searched for valid data with the correct trigger number. The column and row address and the ToT of these hits are serialized and sent to the MCC. The Readout Controller adds a 'start of event' and an 'end of event' word (with error and status bits) to the data stream.

Additional Features

Some of the additional features implemented into FEI to increase the performance and the testability of the chip are mentioned in this section.

1) Testability

All stored bits on the chip can be read back for testing and to check for SEU. A digital injection of hits (after the discriminator) with arbitrary patterns makes it possible to test all locations of the EoC buffers and to check the overflow warning bits. The global 8 bit current DACs used to set global bias conditions can be monitored on a single pin connected to an analogue multiplexer. An analog buffer allows the observation of analog pulses after the preamplifier and after a second stage in the analog pixel part.

2) Measurement of the sensor leakage current

The leakage current compensation circuit in the pixel can provide (if selected) a replica of the leakage current on an analogue bus. A slow 8 bit ADC on the chip is used to measure this current. This feature makes it possible to determine the leakage current of every individual sensor pixel for instance after irradiation.

3) Self Triggering feature

A reliable test of module performance which can be performed in the lab is the exposure of the assembly to a radioactive source. The triggers required to start the readout of hit data can be provided e.g. by a scintillator, but this requires a complicated setup and requires penetrating particles. Low energetic x-ray sources to check the thresholds are excluded with his method. A much simpler method is to use the fast hit-OR signal provided by the analog section to generate a level1 trigger signal after some delay. This 'self-trigger' generator is integrated into the chip so that no external circuitry is required for source measurements.

4) Digital time walk correction

Every hit must be associated to the correct bunch crossing, i.e. the discriminator must not fire later than 25 ns after the charge has been deposited in the sensor. This requirement is difficult to fulfil when hits have small amplitudes just above the threshold. The rise time of the amplifier and the response time of the discriminator then lead to a 'time walk' so that hits just above threshold may be detected too late. The correlation of small amplitude and large time walk is exploited in a digital time walk correction in FEI: The leading edge time stamp is corrected by one if the ToT amplitude is below a programmable cut value. For testing, these 'suspicious' hits can also be written twice into the EoC buffers, once with the nominal, once with the corrected leading edge time stamp. The ToT threshold for this correction is a global, programmable value so that a fine trimming of the ToT-time walk relationship in every pixel is required. This is accomplished by tuning the feedback current with the above mentioned 5 bit pixel DACs.

III. Results

All important features of FEI operate as expected. The supply currents of ~62 mA @ 2 V for the digital part and of ~50 mA @ 1.6 V for the analogue part (nominal settings) are below the baseline values which would be acceptable from the cooling point of view. An equivalent noise charge of ~150 e^- has been measured on the wafer level. This noise increases by ~50 e^- per 100 fF of sensor capacitance and per 10 nA of leakage current as measured on a test chip with appropriate load structures at the preamplifier input. When bump bonded to a module the noise stays below 300 e^-. The initial threshold dispersion of ~ 900 e^- on a bare die can be fine tuned to below 150 e^- (rms) on a module.

Single FEI dies have been irradiated at LBNL and at CERN to above 50 Mrad (the dose accumulated after 10 years of LHC operation) and no significant degradation in the performance (speed, noise, threshold dispersion after tune) has been observed.

Test beam measurements with several fully equipped FEI modules have been performed recently and first results will be available soon.

IV. References

1. D.Barberis et al., The ATLAS silicon pixel sensor, Nucl. Instr. and Meth. A 456 (2001) 217-232.
2. W. Snoeys et al., Layout techniques to enhance the radiation tolerance of standard CMOS technologies demonstrated on a pixel detector readout chip, Nucl. Instr. Meth. A439 (2000) 349-360
3. T. Calin, M. Nicolaidis, R. Velazco, Upset hardened memory design for submicron CMOS technology, IEEE Trans. Nucl. Science, Vol. 43, No. 6, Dec. 1996, pp. 2874-2878