Use of antifuse-FPGAs in the Track-Sorter-Master of the CMS Drift Tube Chambers

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Abstract

The Track-Sorter-Master (TSM) is an element of the on-chamber trigger electronics of a Muon Barrel Drift Tube Chamber in the CMS detector. The TSM provides the chamber trigger output and gives access to the trigger electronic devices for monitoring and configuration.

The specific robustness requirements on the TSM are met with a partitioned architecture based on antifuse-FPGAs. These have been successfully tested with a 60 MeV proton beam: SEE and TID measurements are reported.

I. Introduction

The trigger electronics of a Muon Barrel Drift Tube chamber [1] of the Compact Muon Solenoid (CMS) detector is a synchronous pipelined system partitioned in several processing stages, organized in a logical tree structure and implemented on custom devices (Fig. 1).

The Track-Sorter-Master of the Trigger Server [2] is the system responsible for the trigger output from the chamber and for the trigger interface with the chamber control unit.

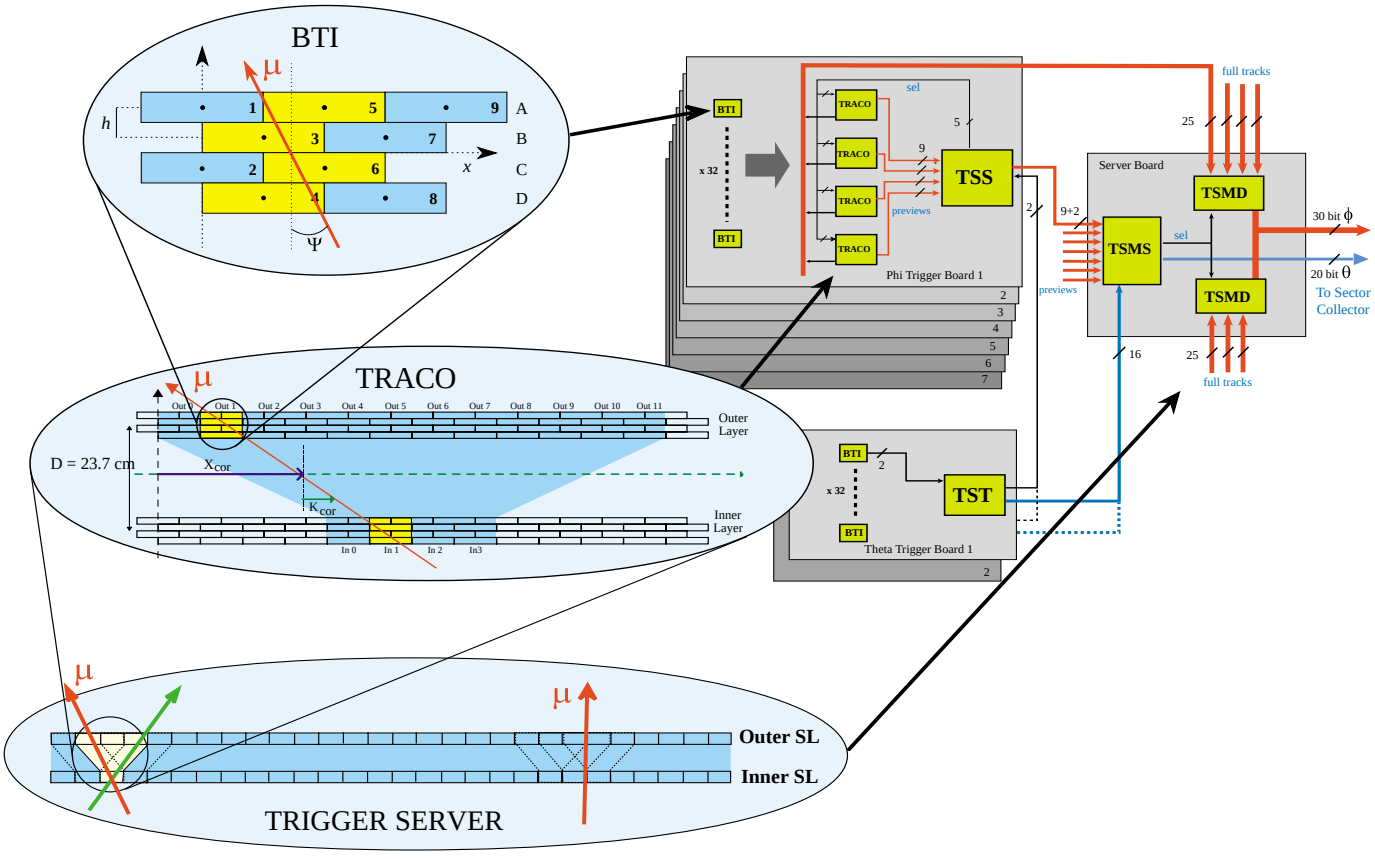

Figure 1: CMS Drift Tube on-chamber trigger electronics overview. The upper right picture, named Server Board, is a block diagram representation of the Track-Sorter-Master system.

Since the TSM system is the bottleneck of the trigger electronics of a muon chamber, a principal requirement it has to fulfil is robustness; it should also be fast in order to minimize the trigger latency.

Moreover, the system should stand the radiation dose expected for 10 years of running of the muon chambers in CMS at the Large Hadron Collider.

In the following we show that this can be achieved with a highly partitioned architecture that utilizes antifuse-FPGAs.

II. Track-Sorter-Master Architecture and Design

A. Architecture

In order to match the robustness requirement, the system is segmented in blocks with partially redundant functionality (Fig. 2). We favour an architecture where the TSM consists of three parts: a Selection (TSMS) block, two Data multiplexing (TSMD) blocks (called TSMD0 and TSMD1, covering half a chamber each). The TSMS receives Preselect Words (PRW) carrying the information of the first stage of sorting performed by the Track Sorter Slave (TSS) units [2]. The TSMDs have as an input the full TRACO data of the track segments selected by the TSSs.

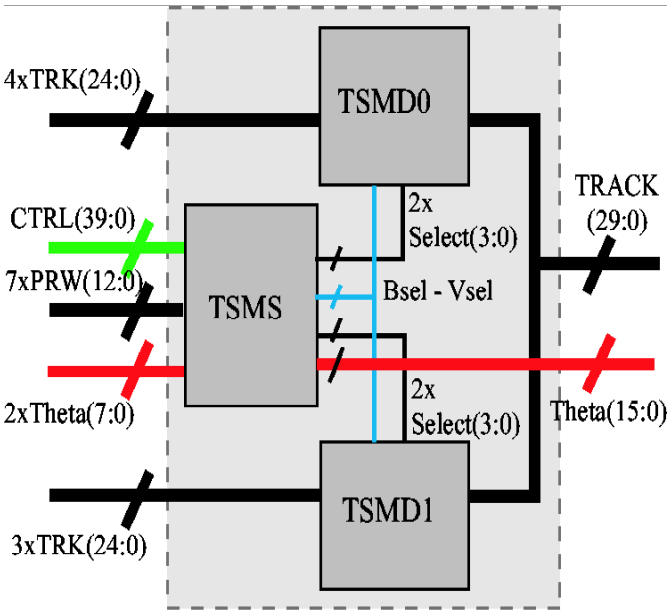

Figure 2: Track-Sorter-Master block diagram. Architecture and I/O signals are shown.

The TSM can be configured into two distinct processing modes:

- Default processing: the TSMS performs as a sorter while the TSMDs act as data multiplexers. The TSMS can select two tracks in TSMD0 or two tracks in TSMD1 or one track each.
- Back-up processing: the TSMS is inactive. Each TSMD performs as sorter and as multiplexer on data from a half chamber. Each TSMD outputs one track.

The Default processing implements the full performance and guarantees that dimuons are found with uniform efficiency along the chamber. In case of failure of one TSMD, the PRWs of the corresponding half chamber are disabled in TSMS sorting, so that full efficiency is maintained in the remaining half chamber.

The Back-up processing mode is activated in case of TSMS failure. It guarantees full efficiency for single muons and for open dimuon pairs (one track in each half chamber).

B. Design

In the hardware design the TSMS, TSMD0 and TSMD1 blocks are implemented as three distinct ICs. Each block has independent power lines. Three separate lines, from the chamber Controller, are used to provide enable signals (nPWRenSort, nPWRenD0 and nPWRenD1) for the power switches. When one IC is powered down, also all I/O lines to the chip are disconnected via bus isolation switches driven with the same enable signals. For this purpose highly reliable switches with very large MTBF are used. Three independent power fault signals are generated and reported to the Controller when an overcurrent condition is detected in the corresponding power net.

The TSM processing configuration can be changed from the Controller by acting directly on the power enable signals. The TSMS also receives the power enable state of the TSMD0 and of the TSMD1, then it can change its processing mode to select two tracks from the same TSMD, when the other TSMD is powered off. Similarly each TSMD receives the power enable state of both the TSMS and the other TSMD, and it can switch to the back-up processing mode when the TSMS is not powered. The system can still run in the extreme scenario of only one functioning TSMD block and its connections undamaged.

The processing mode is selected via configuration registers in all three devices. Registers are also used for the set-up of the sorting and the fake-rejection algorithms. Access to the configuration registers is possible in two independent ways: through a serial JTAG net for boundary scan and through the DT parallel access bus with an ad-hoc protocol, hereafter called Parallel Interface (PI).

Figure 3(a) shows the JTAG net through the three ICs: the net can be configured to run only through the chips that are powered on, using isolation switches controlled via the power enable lines.

Figure 3(b) shows how the PI bus is distributed through the TSM system; each IC has its own TSM address. The PI commands from the chamber Controller are forwarded to the other trigger boards in the same chamber (Fig. 1) through the TSMS. The TSMS gives access to only one trigger board in turn. In case of TSMS failure the trigger boards can still be configured via their individual JTAG nets. The PI utilises the same lines used for propagating the PRW data; the PRW bus is bi-directional.

III. IMPLEMENTATION

A. *Choice of technology*

The most important aspect is the choice of technology in developing the TSMS and TSMD ICs.
There is one TSM system in each DT chamber, that is a total of 250 TSMS and 500 TSMD ICs in the entire muon barrel detector of CMS [1]. This is a too limited production volume for justifying the risk of developing two ASICs

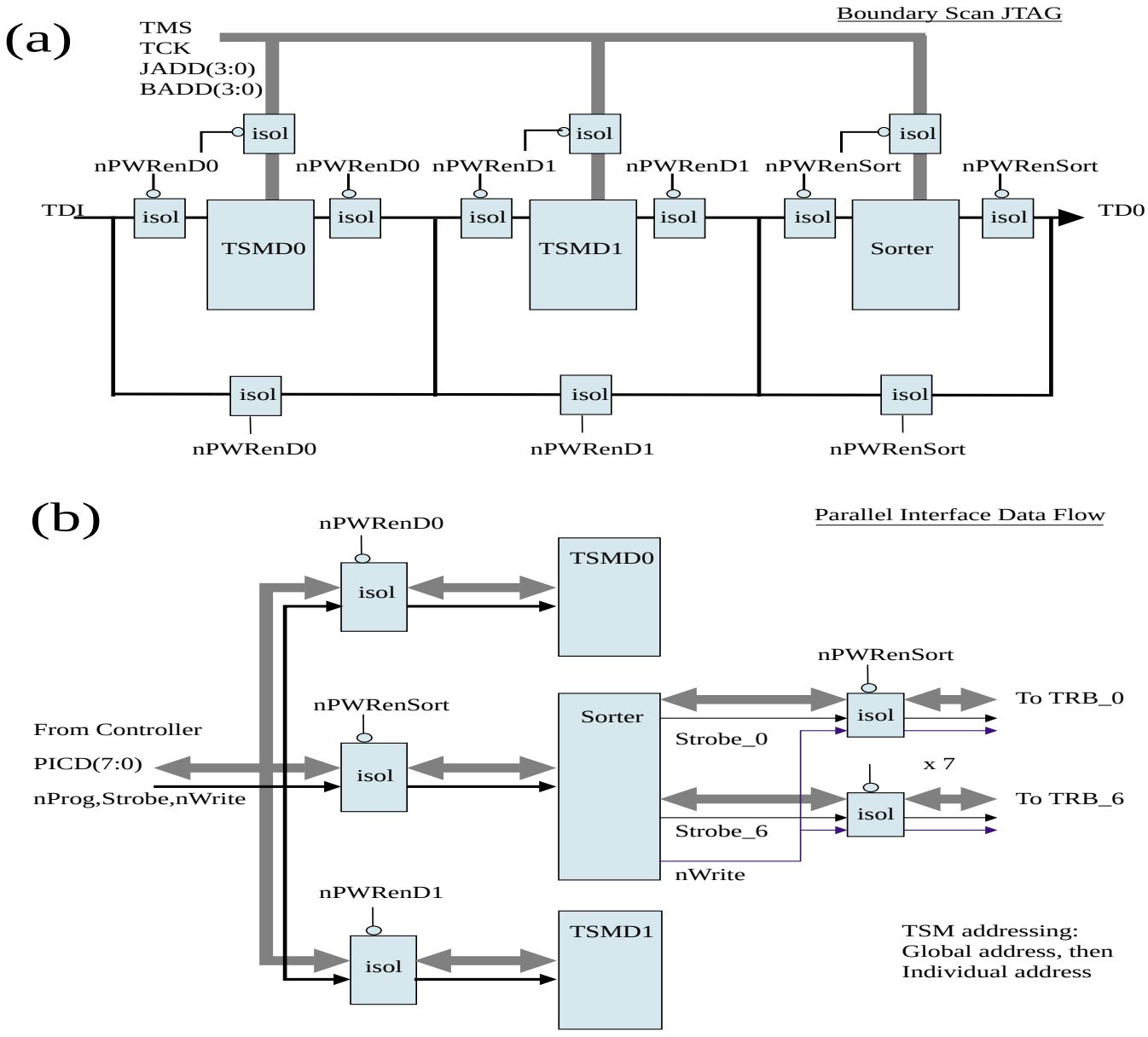

Figure 3: (a) TSM JTAG Net
(b) TSM Parallel Interface Net

The use of FPGAs has two advantages:

- The same type of device can be used for both the TSMS and the TSMD, because the chosen

architecture requires a comparable number of pins for both ICs.

- It leaves flexibility for fine-tuning of the sorting and ghost rejection algorithms.

However standard FPGAs are disfavoured because of their low level of radiation tolerance, which can easily result in erasure and uncontrolled corruption of the programmed logic.

A solution is the antifuse-FPGAs, also called pASICs (programmable ASICs). They are based on silicon antifuse technology: silicon logic modules in a high density array are interconnected using 3 to 4 metal layers where metal-to-metal amorphous silicon interconnect elements (the antifuses) are embedded between the metal layers. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection. Once programmed, the chip configuration becomes permanent, making it effectively like an ASIC.

The Actel A54SX32 [3] device was chosen.

The small dimensions of the board constitute an other design constraint. Therefore, we have built a full-functionality prototype board (Fig. 4) with final dimensions (98x206 mm^2). It has been possible to find a placement of the components that allows efficient routing and good high-frequency behaviour, using six signal layers and a standard 5 mils routing technology. This final prototype is under test.

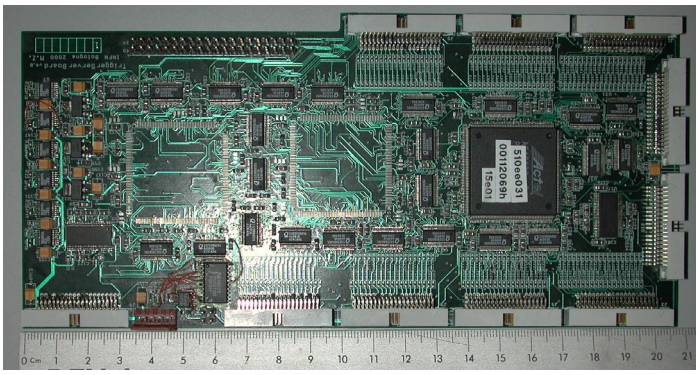

Figure 4: PCB prototype for the Track-Sorter-Master. The larger chip on the right side is an A54SX32 programmed as TSMS. Places to host both TSMDs are visible.

IV. IRRADIATION TEST

A. Program of tests

The Actel A54SX chips have been chosen for building the TSM after a test of their radiation tolerance has been performed. Samples have been exposed in the 59 Mev proton beam of the Cyclotron Research Centre (CRC) at the Universite Catholique de Louvain (UCL), in Louvain-la-Neuve, Belgium, in October 2000. At this energy 10^{10} protons/cm^2 correspond to a dose of 1.4 krads.

B. Test Setup

Four pASICs, each implementing a 450-bit register, refreshed and monitored at 1 MHz, have been irradiated up to 40 krads/chip (one of them up to 70 krads). The register size of 450 bits is similar to that of registers in both the TSMS and TSMD chips.

Figure 5 shows the set-up used for these tests. Pattern Unit (PU) [4] is a high-throughput VME board, acting as pattern generator and as read-out module.

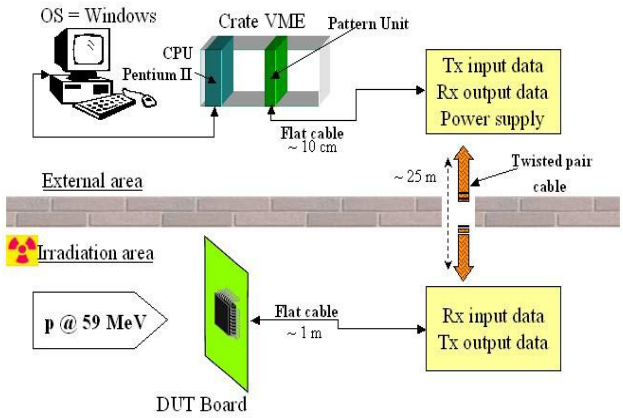

Figure 5: Irradiation test set-up.

C. Results

There has been no failure and no latch-up.

The Total Irradiation Dose (TID) result is summarised in figure 6: no significant increase in current is observed for doses well above that of a few krads expected for the CMS barrel muon chambers in 10 years of LHC operation [5].

We have observed one Single Event Upset. The event has been recorded and studied off-line. The 450 bit register dump shows that in the event about 1/3 of the flip-flops have changed state, with no obvious correlation in pattern. With the help of Actel CAD tools, we have inferred that most probably the internal clock distribution to the register cells has failed.

Because of this, we quote a SEU cross-section measurement per chip instead of per bit. According to the

procedure established in [5], we can use this measurement for estimating the SEU rate in CMS.

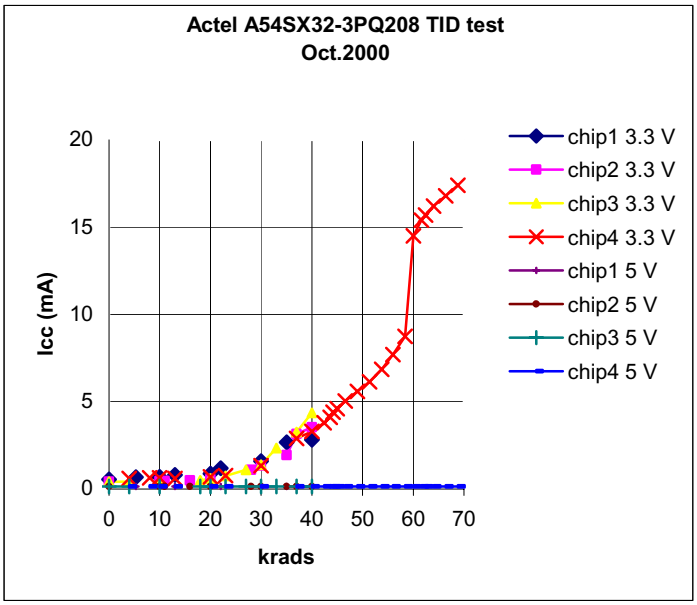

Figure 6: Irradiation test set-up.

With one observed event and a total fluence of 1.4 10^{12} protons/cm^2, we calculate a SEU cross-section upper limit (at 90% c. l.) of

$\sigma_{SEU} < 2.9\ 10^{-12}$ cm^2 per A54SX32 chip of the TSM.

The flux of neutrons with energy exceeding 20 MeV is expected to be of at most 10^9 neutrons/cm^2 in the CMS muon barrel region [5] in 10 years of LHC running.

Since the complete TSM system will consist of 750 A54SX32 chips, the expected SEU rate is

$R_{SEU} < 2.2$ events in 10 years of DT chambers data taking.

Full functionality is recovered when refreshing the registers.

V. Conclusions

The Track-Sorter-Master system of a Muon Barrel Drift Tube chamber in CMS performs the final selection of muon track segments and provides the chamber trigger output. It is also the interface between chamber control unit and chamber trigger electronics.

The core functionality of the Track-Sorter-Master will be implemented with antifuse FPGAs Actel A54SX32.

With this choice we have enough design flexibility for implementing a highly robust partitioned architecture, together with high processing speed and radiation tolerance.

Tested with a 59 MeV proton beam antifuse-FPGAs show good tolerance to high radiation doses of up to 50 Krads and high thresholds for Single Event Upsets (SEU).

VI. References

[1] CMS Collaboration, The Level-1 Trigger, Technical Design Report, CERN LHCC 2000-038, 15 December 2000, section 9

[2] G.M.Dallavalle, I.D'Antone, S.Marcellini, A.Montanari, F.Odorici and G.Torromeo, Proceeedings of the Fourth Workshop on Electronics for LHC Experiments, CERN LHCC 98-36 (1998) 294

[3] www.actel.com/user/html/databook99.html: see "SX Family FPGAs"

[4] G.M.Dallavalle, I.D'Antone, I.Lax, A.Montanari and F.Odorici, Proceeedings of the Fourth Workshop on Electronics for LHC Experiments, CERN LHCC 98-36 (1998) 291

[5] M.Huhtinen and F.Faccio, Nucl. Instr. and Meth. A-150 (2000) 155; see also CMS Collaboration, The Muon Project, Technical Design Report, CERN/LHCC 97-32, CMS TDR 3, 15 December 1997; see also M.Huhtinen, CMS COTS Workshop, Nov.1999