Radiation test and application of FPGAs in the Atlas Level 1 Trigger

Valerio Bocci
INFN Sezione di Roma

7th Workshop on Electronics for LHC Experiments

Stockholm, Sweden, 10-14 September 2001
Presentation overview:

• Atlas RPC radiation environment.
• Virtex FPGA structure.
• SEU test in Virtex logic.
• SEU test in Virtex configuration memory.
• TID test.
• Annealing test.
• Continuous check and recovery inside the system.
Atlas RPC muon system location and radiation levels

<table>
<thead>
<tr>
<th>Location</th>
<th>Zmin (cm)</th>
<th>Zmax (cm)</th>
<th>Rmin (cm)</th>
<th>Rmax (cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>BMF</td>
<td>63.1</td>
<td>872.2</td>
<td>839.1</td>
<td>847.1</td>
</tr>
<tr>
<td>BML</td>
<td>15</td>
<td>966</td>
<td>750.6</td>
<td>758.6</td>
</tr>
<tr>
<td>BMS</td>
<td>13.5</td>
<td>945.5</td>
<td>839.1</td>
<td>847.1</td>
</tr>
<tr>
<td>BOF</td>
<td>60.8</td>
<td>1267.9</td>
<td>1035.5</td>
<td>1043.5</td>
</tr>
<tr>
<td>BOL</td>
<td>15</td>
<td>1225.2</td>
<td>985.3</td>
<td>993.3</td>
</tr>
<tr>
<td>BOS</td>
<td>1</td>
<td>1383.2</td>
<td>1025.8</td>
<td>1033.8</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Location</th>
<th>$\text{SRL}_{\text{ud}}$ (Gy 10y$^{-1}$)</th>
<th>$\text{SRL}_{\text{see}}$ (&gt;20 MeV h cm$^{-2}$ 10y$^{-1}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>BMF</td>
<td>3.02E+00</td>
<td>4.69E+09</td>
</tr>
<tr>
<td>BML</td>
<td>3.04E+00</td>
<td>5.65E+09</td>
</tr>
<tr>
<td>BMS</td>
<td>3.03E+00</td>
<td>4.73E+09</td>
</tr>
<tr>
<td>BOF</td>
<td>1.19E+00</td>
<td>4.08E+09</td>
</tr>
<tr>
<td>BOL</td>
<td>1.33E+00</td>
<td>4.21E+09</td>
</tr>
<tr>
<td>BOS</td>
<td>1.26E+00</td>
<td>4.10E+09</td>
</tr>
</tbody>
</table>

V.Bocci    LEB 2001    Stockholm, Sweden, 10-14 September 2001
Xilinx Virtex 2.5V device

Fast, high-density
Field-Programmable Gate -
- System performance up to 200 MHz
Built-in clock-management circuitry
- Four dedicated delay-locked loops (DLLs) for advanced clock control
- Four primary low-skew global clock distribution nets,

Each Block SelectRAM is a fully synchronous dual-ported 4096-bit RAM with independent control signals for each port. The data widths of the two ports can be configured independently.

Built-in bus-width conversion.

<table>
<thead>
<tr>
<th>Device</th>
<th>System Gates</th>
<th>CLB Array</th>
<th>Logic Cells</th>
<th>Maximum Available I/O</th>
<th>Block RAM Bits</th>
<th>Maximum SelectRAM™ Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>XCV200</td>
<td>236,666</td>
<td>28x42</td>
<td>5,292</td>
<td>284</td>
<td>57,344</td>
<td>75,254</td>
</tr>
</tbody>
</table>

V.Boci LEB 2001 Stockholm, Sweden, 10-14 September 2001
SEU in FPGAs devices

- FPGA logic cross section.
- FPGA configuration cross section.
- FLASHProm SEU cross section.

Asic                  FPGA
1 flip-flop   ->   30 flip-flop

Mitigation circuits for SEU
Xilinx XCV200 and Flashprom 18V02 Louvain Test Board
Test of logic SEU circuit:
The Xilinx XCV200 was configured as 2048 Shift register with a “101...010” pattern and SEU detection circuit plus error correction.
Virtex has been irradiated with 60 Mev protons in the Louvain facility.
Test results from our first Louvain campaign

Logic SEU
5 events /6.14*10^{10}
(60 MeV protons)
\textbf{Xsect/bit=3.98*10^{-14}}

Configuration
SEU events
23 events/6.14*10^{10}

V.Bocci  LEB 2001  Stockholm, Sweden, 10-14 September 2001
Monitors of XCV200 configuration using multiLINX cable

The MultiLINX device with a USB interface increases communication speed up to 12 Mbits/s, thus reducing download and verify times by a factor of 120X compared to JTAG cable. We download the Xilinx with the shift register configuration and then monitor the number of wrong configuration bits after a given fluence of 60 Mev protons.

V. Bocci  LEB 2001  Stockholm, Sweden, 10-14 September 2001
Test results from second Louvain campaign

\[ y = 8 \times 10^7 x \]
\[ R^2 = 0.9991 \]

V. Bocci  
LEB 2001  
Stockholm, Sweden, 10-14 September 2001
FlashProm SEU test

Xilinx 18v02 FlashPROM:

- In-system programmable 3.3V PROMs for configuration of Xilinx FPGAs
- Endurance of 10,000 program/erase cycles
- Program/erase over full commercial/industrial voltage and temperature range
- IEEE Std 1149.1 boundary-scan (JTAG) support
- Simple interface to the FPGA; could be configured to use only one user I/O pin
- Cascadable for storing longer or multiple bitstreams
- Dual configuration modes
  - Serial Slow/Fast configuration (up to 33 MHz)
  - Parallel (up to 264 MHz)
- Low-power advanced CMOS FLASH process
- 5V tolerant I/O pins accept 5V, 3.3V and 2.5V signals.
- 3.3V or 2.5V output capability
- Available in PC20, SO20, PC44 and VQ44 packages.
- Design support using the Xilinx Alliance and Foundation series software packages.
- JTAG command initiation of standard FPGA configuration.

After an integrated flux over 4 devices of $8 \times 10^{11}$ protons/cm$^2$ @ 60 Mev

**We did not observe any SEU.**

At about $2 \times 10^{11}$ protons (28 Krad) the programming feature does not work.

$X_{\text{section}}/\text{bit} < 1.25 \times 10^{-18}$ cm$^2$

V.Bocci                   LEB 2001                   Stockholm, Sweden, 10-14 September 2001
387 Rad/min Co$_{60}$ Gamma ray source in the Istituto Superiore di Sanita’ Rome
Flashprom 18V02 Co$_{60}$ irradiation

Atlas RPC worst case total dose including safety factors
4.2Krad=302 Rad*4(SF$_{sim}$)*3.5(SF unknown batch)

The programming function does not work

V.Bocci                                        LEB 2001             Stockholm, Sweden, 10-14 September 2001
Flashprom 18V02 one week @ 100 °C annealing

V.Bocci
LEB 2001
Stockholm, Sweden, 10-14 September 2001
XCV200 Co\textsubscript{60} irradiation

![Graph showing XCV200 Co\textsubscript{60} irradiation with annotations for Program & Readback and Stop working.]

V. Bocci  
LEB 2001  
Stockholm, Sweden, 10-14 September 2001
XCV200 $\text{Co}_{60}$ irradiation

![Graph showing XCV200 and Xilinx2 irradiation response with annotations: Stop working, Program & Readback.]
XCV200 Co$_{60}$ irradiation

V.Bocci
LEB 2001
Stockholm, Sweden, 10-14 September 2001
XCV200 Co$_{60}$ irradiation

XCV200
Xilinx1.2 same program
Xilinx3 only jtag running

4.2Krad

Stop working

Dose (Krad)

0 10 20 30 40 50 60 70 80 90 100 110 120 130

I(ma)
Xilinx XCV200 annealing one week @ 100 °C

V. Bocci

LEB 2001

Stockholm, Sweden, 10-14 September 2001
Low $p_T$ PAD board

- Pad logic chip, which covers a region $?\times? = 0.2\times0.2$, associates muon candidates with a region $?\times?=0.1\times0.1$ (RoI);
- It selects the higher triggered track in the Pad;
- Pad logic chip solves overlap inside the Pad;
- The information of two adjacent CMAs in the $?_{1}$ projection, and the corresponding information of the two CMAs on the $?_{2}$ projection, are combined together in the low-$p_T$ Pad logic board;
- The four low-$p_T$ CM boards and the corresponding PAD logic board are mounted into a single PAD box, on the outermost side of the RPC2 detector;
Location of the XCV200 inside the LVL1 muon Trigger
XCV200 in Atlas muon environment

Device $X_{\text{sect}} = 1.25 \times 10^{-8} \text{ cm}^2$
6.25 SEUs in one year
SEU with SF = $6.25 \times 5(SF_{\text{sim}}) \times 4(SF_{\text{lot}}) = 125$ in one year

Device $X_{\text{sect}} < 5 \times 10^{-12} \text{ cm}^2$

FPGA XCV200

Flash 1.3 Mbits

8 bits x 33 Mhz SelectMap
~ 5 ms configuration time

JTAG (Max 8 Mbit/s 163 ms)
@ 500Kbits/s 2.6 sec

DCS node

<0.3 Rad /10 yr Atlas muon
Atlas muons = $5 \times 10^8$ hadrons/cm$^2$ yr

==> 50 hadrons/cm$^2$ sec

V. Bocci  LEB 2001  Stockholm, Sweden, 10-14 September 2001
PAD board with TTCrx ELMB XCV200 and Optical Link
Configuration SEU recovery system

FPGA

FlashRom

Local Task

CAN Node

• Continuos readback from the ? controller in the CAN node
• init in case of wrong configuration.
• Test of init fail after configuration

SPI

CRC TABLE

FLASHROM

CanMessages:
-> life guarding
-> wrong xlnx config
-> wrong init
<= program Flashrom

V. Bocci

LEB 2001 Stockholm, Sweden, 10-14 September 2001
FPGA initialization

INIT

LOAD Configuration From Flash

OK ? NO

YES

Background read-back

CAN MSG wrong Flash

ERASE & PROGRAM FLASH ROM

CAN MSG wrong Configuration

OK

NO

FPGA programming using JTAG

Local task
Bandwidth consuming task
CAN messages

V.Bocci
LEB 2001
Stockholm, Sweden, 10-14 September 2001
Readback data structure

- Readback and mask single frame (2186 frames in XCV200)
- CRC computation and comparison with the stored value in the SPI Flashrom
- Estimated time needed to check all frames <30 sec

<table>
<thead>
<tr>
<th>Device</th>
<th>CL Frames</th>
<th>Bytes per Frame</th>
<th>Frame Bytes</th>
<th>Pad Bytes</th>
<th>Readback Bytes</th>
</tr>
</thead>
<tbody>
<tr>
<td>V200</td>
<td>2186</td>
<td>60</td>
<td>140640</td>
<td>8016</td>
<td>167464</td>
</tr>
</tbody>
</table>

V.Bocci LEB 2001 Stockholm, Sweden, 10-14 September 2001
Conclusions

• XCV200 Irradiation with protons and gamma was performed.

• The SEU logic cross section is similar to other devices with 0.25 μm technology.

• The SEU coming from the configuration memory complicate the problem of one order of magnitude respect to the pure Asic design.

• The TID tolerance is more than LVL1 maximum requirements.

• The immunity of Flashprom technology to SEU can be used for fast reprogramming of Xilinx configuration on board.

• The availability of CPU power from DCS node can be used to continuously check the Xilinx program.