Studies for a Detector Control System for the ATLAS Pixel Detector

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Abstract

For the ATLAS experiment at the LHC, CERN, it is planned to build a pixel detector containing around 1750 individual detector modules. The high power density of the electronics requires an extremely efficient thermal management system: an evaporative fluorocarbon cooling system has been chosen for this task. The harsh radiation environment presents another constraint on the design of the control system, since irradiated sensors can be irreparably damaged by heating up. Much emphasis has been placed on the safety of the connections between the cooling system and the power supplies. An interlock box has been developed for this purpose. We report on the status of the evaporative cooling system, on the plans for the detector control system and on the irradiation studies of the interlock box.

I. INTRODUCTION

The pixel detector is the component of the ATLAS inner tracker closest to the interaction point. From the monitoring point of view, the base unit is a detector module consisting of a pixelated silicon sensor, with 16 bump-bonded front end readout chips. A flexible hybrid circuit is attached and carries a "Module Controller Chip" which organizes data transmission from the module via a bi-directional optical link. The optical link is located close to the detector module and contains a VCSEL (vertical cavity semiconductor laser) and a PIN diode, together with their corresponding transceiver chips "VDC" and "DORIC" {[1], figure (1)}. Besides the voltages, necessary to drive the different electronic components, one temperature sensor per module must be handled by the detector control system (DCS). The detector modules are glued on the different support structures ("staves" in the barrel part, disks in the "end-caps") which contain the cooling pipes necessary to remove the heat dissipated by the electronics.

The following three sections describe the three main components of the pixel DCS: the cooling system, the power supplies and the temperature monitoring and interlock system. Emphasis is put on the characterization of the hardware. Wherever possible we try to use ATLAS standard components, especially the ELMB (Embedded Local Monitor Box)[2]: a multi purpose acquisition and control unit, using the CAN fieldbus and developed by the ATLAS DCS group. Section V contains an overview of the whole Pixel DCS and reports on the first steps in the implementation of a SCADA ["Supervisory, Control and Data Acquisition"] system. The summary in section VI includes an outlook on future plans.

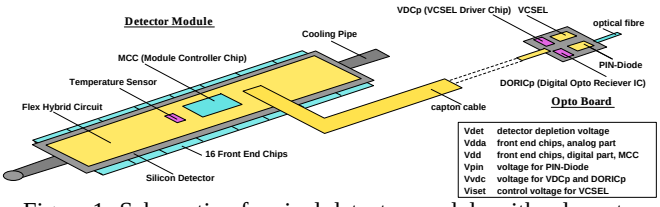

Figure 1: Schematic of a pixel detector module with relevant components of the Detector Control System

II. THE COOLING SYSTEM

A. The Challenge

For a ten-year operational lifetime in the high radiation field close to the LHC beams, the silicon substrates of the ATLAS pixel detectors must operate below ~ -6 °C with only short warm-up periods each year for maintenance. Around 15 kW of heat will be removed through ~ 80 parallel circuits, each cooling a series pair of pixel barrel staves (208 or 290 W) or disk sectors (96 W). Evaporative per-fluoro-n-propane (C_3F_8) cooling [3] has been chosen since it offers minimal extra material in the tracker sensitive volume (flow rates 1/20 those in a monophase liquid system), with a refrigerant that is non-flammable, non-conductive and radiation resistant. Since the pixel stave and disk sector "local supports" are of the lowest possible mass composite construction, detectors can exhibit a very rapid temperature rise (~ 5 Ks^{-1}) in the event of a loss of coolant or cooling contact. A rapid thermal interlock with the module power supplies is therefore indispensable. Thermal impedances within the local supports require C_3F_8 evaporation in the on-detector cooling channels at ~ -20 °C for a silicon operating temperature of ~ -6 °C.

B. The Recirculator and Principle of Operation

A large scale (6 KW) prototype circulator (Fig. 2) can supply up to 25 parallel cooling circuits, through interconnecting tubing replicating the lengths and hydrostatic heat differences expected in the final installation in the ATLAS cavern.

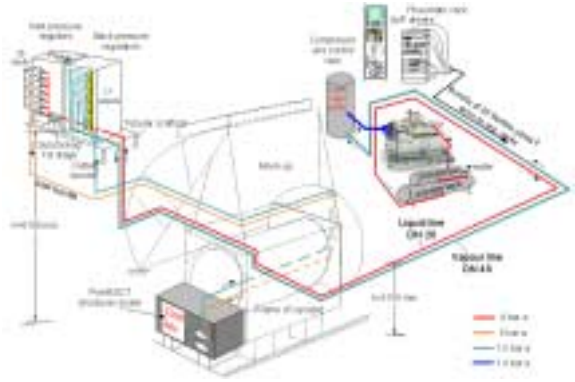

Figure 2:
Schematic of Prototype Evaporative Recirculator

It is centred on a hermetic, oil-less piston compressor[1] operating at an aspiration pressure of ~1 bar_{abs} and an output pressure of ~10 bar_{abs}. Aspiration pressure is regulated via PID variation of the compressor motor speed from zero to 100%, based on the sensed pressure in an input buffer tank. C_3F_8 vapor is condensed at 10 bar_{abs} and passed to the detector loads in liquid form. A detailed description of the principle of operation is given in ref [4].

In the final installation, liquid will be distributed, and vapor collected, in fluid manifolds on the ATLAS service platforms. This zone will be inaccessible to personnel during LHC running, with local radiation levels and magnetic fields that exceed acceptable levels for a wide range of commercial control electronics. Local regulation devices will be pneumatic: in each cooling circuit, coolant flow rate will be proportional to the output pressure of a "dome-loaded" pressure regulator[2], placed ~ 25 m upstream of an injection capillary, piloted by analog compressed air in the range 1-10 bar_{abs} from an I2P (4-20mA input) or E2P (0-10V input) electro-pneumatic actuator[3]. Actuators will receive analog set points from DACs, which will either be commercial control components[4], or an adjunct to the ATLAS ELMB monitor and control card [2]. Circuit boiling pressure (hence operating temperature: at 1.9 bar_{abs}, C_3F_8 evaporates at –20°C) will be controlled by a similarly piloted dome-loaded backpressure regulator[5].

C. PID Regulation of Coolant Mass Flow

Coolant flow in each circuit will be PID-regulated to maintain the temperature on a NTC sensor on the exhaust 50 cm downstream of a cooled detector element ~> 10 °C above the C_3F_8 evaporation temperature. In this way it is not necessary for the cooling control system to detect how many detector modules on a cooling circuit are powered (or their instantaneous power dissipation).

A PID algorithm has been implemented directly [4] in a microcontroller chip[6] of the same family as that used[7] for system programming and monitor functions in the ATLAS ELMB. The results indicated that with proportional flow control, stability in temperature of -6 ± 1 °C on remaining powered modules is achievable, with > 90 % of the supplied C_3F_8 liquid evaporated in the on-detector tubing. In setting up the PID parameters, care was needed to ensure that the lower pressure limit was not less than the saturated liquid pressure at the C_3F_8 liquid injection temperature.

The tubing of the cooling circuits requires insulation (and possibly local surface heating in certain critical locations) to safely traverse the electrical services of other ATLAS sub-detectors, which are located in an ambient air atmosphere with ~ 14 °C dew point.

The results also demonstrated PID colant flow regulation allows a relatively simple insulation scheme to maintain the outer surface of the exhaust tubing above the local dew-point, reducing the insulation volume required in the extremely restricted service passages.

A DAC adjunct is under design for the ATLAS ELMB [2]. This would allow PID flow regulation through control loops from the ELMBs with one or more PID channels in the on-board microcontroller of each ELMB. While it is also possible to implement a software PID algorithm for each circuit in the final ATLAS SCADA software, it is not known at this stage whether the reaction time will be fast enough for our application.

III. THE POWER SUPPLY SYSTEM

Six different voltages are necessary for the operation of each pixel detector module, (figure 1). These must supply a depletion bias of up to 700 V and five low voltage loads varying between low power consumption to two which draw 2-5 Amperes. In order to support the ATLAS grounding scheme, all voltages will be floating.

We aim to use a coherent power supply system which accommodates these diverse requirements and has a high level of local intelligence. A system able to make decisions autonomously - not relying on the functionality of the network - will reduce field-bus traffic and will enhance the safety of the detector. Error conditions (including over-current) will be handled in the power supply system, leaving recovery procedures to the operator or supervisory detector control station. The demand for significant local functionality implies the location of the system in an radiation-free environment.

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[1] Model QTOX 125 LM ; Mfr: Haug Kompressoren CH-9015 St Gallen, Switzerland

[2] Model 44-2211-242-1099: Mfr: Tescom, Elk River MN 55330, USA

[3] Model PS111110-A: Mfr Hoerbiger Origa GmbH, A-2700 Wiener-Neustadt, Austria: Input 0-10V DC, Output pressure 1-11 bar_{abs}

[4] Model 750-556: Mfr Wago GmbH, D32423 Minden, Germany controlled through Model 750-307 CAN Coupler

[5] Model 26-2310-28-208: Tescom Corp

[6] AT90S8515; Mfr: ATMEL Corp, San Jose CA 95131, USA: programmed from C via GNU toolkit

[7] ATMEL ATmega103 128k RISC flash μcontroller

For redundancy and grounding considerations, we require a high granularity of power distribution, with a total of ~ 4000 separate channels. In order to handle this large number of channels efficiently and to speed up access, a power supply system is needed which offers the grouping of channels according to the characteristics of the detector and its installation: so called multi-voltage "complex channels" will be formed to power each pixel module. This is also required by the design of our interlock system: a single interlock signal should simultaneously turn off all power supplies to a module.

As the front end chips of the pixel detectors are fabricated in a 0.25 µm deep submicron technology, they are very sensitive to transients. First measurements with a prototype power supply system have shown that line regulators are required. These represent an additional object for the DCS. Their location must be close to the detector, setting a specification for their radiation hardness. The LHC4913[8] is a possible candidate to meet our requirements, and its use is presently under investigation.

IV. Temperature Monitoring and Interlock System

A. Principle

Due to the great influence of the operating temperature on the longevity of the detector, each detector module is equipped with its own temperature sensor. Inaccessibility during long periods of one year or more requires a reliable and robust solution for the temperature measurement: we have chosen a method based on resistance variation. The information from the sensor will be led to the ADC channels of the ELMB for data logging. In parallel, the signal will be fed to an interlock box, which compares it to a reference value and creates, in the case of excessive deviation, a hardwired logical signal which can be used for direct action on the power supplies. This solution protects the detector against risks associated with latch-up, de-lamination of a particular module from its cooling channel or failure of coolant flow to a particular parallel cooling circuit.

B. Choice of the Temperature Sensor

The very limited space requires a component available in a SMD 0603 package, and which can be read via a two wire connection, implying the need of a sensor in the 10 kΩ range. A relatively large change of the resistance per Kelvin reduces the requirements on the precision of the electronic circuit. In order to avoid a calibration of each individual channel, we have been searching for a resistor with small tolerance limits.

Operation in a magnetic field of up to 2.6 T and at a radiation dose of up to 500 kGy (corresponding to 10 years of operation in ATLAS), are pre-requisites. For this reason the package material of the sensor was also taken into consideration.

We found that the requirements listed above were best met by a 10 kΩ NTC resistor with a relative change of its resistance of 4 % per Kelvin[9], available with 1 % tolerance at 25 °C. The type 103KT1608-1P from Semitec is additionally available in a glass coated package.

C. The Interlock Box

Since the interlock box is so closely related to the safety of the detector, we aimed at a pure hardware solution, which should not rely on any initialization via software or multiplexing. The interlock box should be able to work completely independently from other equipment. In addition to module heat up other error conditions including a broken cable or temperature sensor and a short circuit must also cause the setting of the interlock signal. Negative TTL logic is employed.

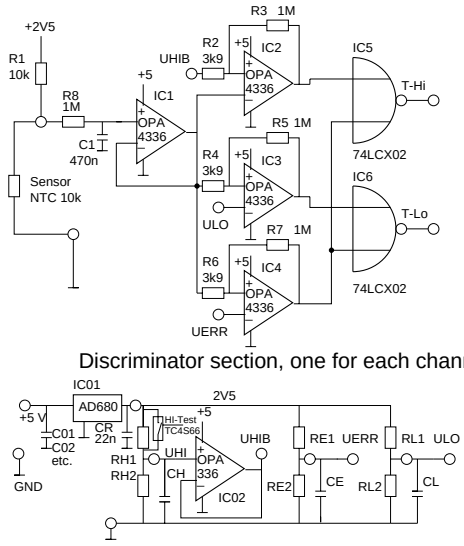

Figure 3: Electrical Schematic of the Interlock Box

In order to reduce the influence of noise, a hysteresis of ~1 K is required between the setting of the alarm signal and its reset. A precision of +/- 1° K is required for the complete chain of temperature sensor, cables and interlock box therefore an accuracy for the interlock circuit alone of < 0.5 K is adequate.

Figure 3 shows the realization of the interlock circuit. A clean reference voltage is created by the reference section. The signal from the NTC is then compared to different thresholds, the op-amps acting as discriminators. The following NOR-gates create a pattern of two bits, representing the different error condition combinations mentioned above.

Several studies [4] have demonstrated that the electrical performance of the circuit is in good agreement with the expected error, which is composed of the error of interlock circuit, caused by the tolerances of the components, of ± 0.2 K and of the tolerances of the NTC of ± 0.3 K (depending on the temperature).

[8] developed by ST Microelectronics (Catania, Italy) in the framework of the RD 49 project, CERN

[9] 10 kΩ @ 25°C, $t(K)=1/(9.577E\text{-}4+2.404E\text{-}4\ln(R)+2.341E\text{-}7\ln(R)^3)$. Mfr: Ishizuka Electronics Co. 7-7 Kinshi 1-Chome, Sumida-ku, Tokyo 130-8512, Japan

D. Irradiation Results on the Interlock Box

As the location of the interlock box will be the ATLAS experimental cavern, the radiation tolerance of all its components must be investigated. Three types of possible problems must be studied in order to qualify the electronics: damage due to ionising ("total ionising dose": TID) and non ionising radiation ("non-ionising energy loss": NIEL) and single event effects (SEE). The expected simulated radiation levels are given in [5]. In order to determine the "radiation tolerance criteria", several safety factors are added, table 1 summarizes them for the interlock box based on the calculations described in [5].

Table 1: "Radiation tolerance criteria" for the Interlock Box

	10 years operation in ATLAS
RTC_{TID}	93 Gy
RTC_{NIEL}	4.8 10^{11} n/cm^2 (1 MeV)
RTC_{SEE}	9.22 10^{10} h/cm^2 (> 20 MeV)

As a pre-selection 3 irradiation campaigns were performed:

- TID studies with a 2.10^4 Ci Co- 60 source;
- A neutron irradiation at the CEA Valduc[10] research reactor with an energy range up to a few MeV with maximum intensity at 0.7 MeV;
- SEU studies at the 60 MeV proton beam of UCL[11].

Usually five devices were irradiated per campaign. During all irradiation tests the components were powered, monitored and checked online for performance and power consumption. For the study of single event effects additionally a special program was developed to monitor the complete circuit for transients or other temporary changes in the output. During the first TID campaign, the first selected NOR-gate (type CD74HC02M[12]) showed severe problems, manifested by an increase of the power consumption. Several further NOR-gates were tested [6]. It was found that the radiation robustness depended not only on the logic family and the manufacturer, but also on the input pattern sent to the device during the irradiation. We found that the MC74LCX02D[13] best met our requirements.

Table 2: Components of the Interlock Box, which passed all three irradiation tests

	Selected Device
Op-Amp	OPA336N
4 fold Op-Amp	OPA4336EA
NOR-Gate	MC74LCX02D
Voltage reference (2.5 V)	AD680JT
Voltage regulator (3.3 V)	LE33CZ
Analog switch	TC4S66
Capacitors	Ceramicmulti-layer, Epcos

As the offset voltage of the op-amp is critical to the accuracy of the circuit (1 mV corresponds to 1/20 K) this quantity was measured for several input voltages. Figure 4 shows a typical result, indicating that no deterioration is expected. The colored band represents the acceptable variation in our application. All other devices showed no problems, either during or after irradiation. Table 2 summarizes the components which finally passed the three irradiation tests.

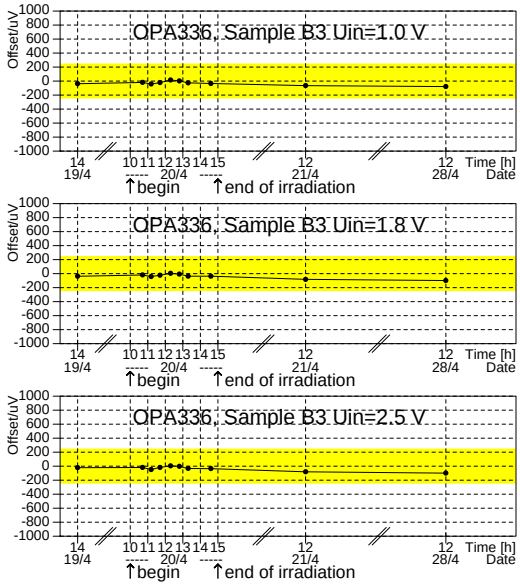

Figure 4: Offset Voltages of the OPA-336 (TID: 100 Gy)

E. The Interlock System

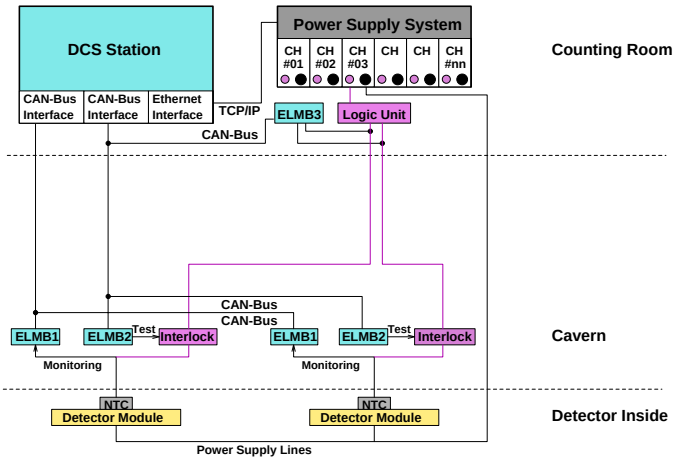

Figure 5: Schematic of the Temperature Monitoring and Interlock System

Figure 5 shows the complete temperature and interlock chain. The signal from the temperature sensor is split between interlock box and ELMB. Information from two interlock channels are combined by the logic unit, as one power supply channel serves two detector modules. In parallel, the digital information from the ELMB is sent to the DCS station via the CAN-Bus for data logging. Additionally, another ELMB monitors the interlock bit pattern. A third ELMB can be used

[10] CEA, Centre de Valduc, F21120 Is-sur-Tille, France
[11] Université Catholique de Louvain, B1348 Louvain-la-Neuve, Belgium
[12] Texas Instruments, USA; www.texas-instruments.com
[13] ON Semiconductors, USA ; www.onsemi.com

to send test signals to the interlock box. This remote test possibility is necessary because the equipment is not accessible during data taking periods. The power consumption of the Interlock Box is also monitored by this third ELMB since an increase in the supply current can indicate problems due to irradiation.

V. The Pixel Detector SCADA System

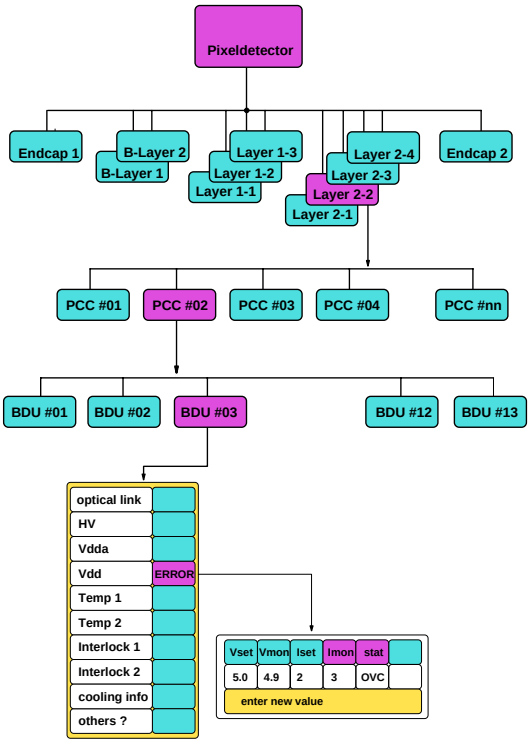

Figure 6: Organization of the Pixel Detector Elements inside the SCADA System

Besides the hardware components described in the previous three sections, the temperature management system (see figure 5) will also be applied for the control of the opto boards (see figure 1), as the performance of irradiated VCSELs will decrease if their temperature exceeds 20 °C. The temperatures of the regulators located in the supply cabling and their input and output voltages and currents are further parameters to be monitored.

Following the recommendations for the ATLAS experiment we have started to implement the SCADA system for the control of the pixel detector using the PVSS commercial software product[14].

Our first studies with PVSS are following geographically oriented structures, where all information relevant for one detector unit is given simultaneously, since this helps to trace and analyse problems. Figure 6 shows how the different levels of the tree structure can be arranged. Following the different levels one can find out in which part of the detector a problem has arisen. As the distribution of the high and low voltages is done with granularity two, from the DCS point of view the smallest unit DCS can act on contains 2 modules - forming a "base detector unit". All other information relevant to the status of a detector module (temperature, status of the related opto link and interlock, etc.) must be available on this level. Information on the status of the cooling system and the readout chain will be supplied via the "event manager".

We have started to implement PVSS version 2.11.1 on a windows NT platform. In this development system we use two OPC servers (OLE for Process Control), one communicating via CAN-Bus to the ELMB which monitors the hardware, and the other handling communication with the power supplies. With this system we have begun to implement a few BDUs, from which larger systems can be composed.

VI. Summary

The requirements of the pixel detector have made specific developments necessary for the hardware components of the DCS. A cooling system using the evaporation of C_3F_8 fluorocarbon has been developed and will be used for the ATLAS pixel and SCT detectors. Control of coolant flow in each circuit via PID regulation has been demonstrated and is being implemented in a 25-channel demonstrator. For the temperature management system, a possible solution is found based on the interlock box and the ELMB. The design of the interlock box uses standard electronic components, which helps to reduce its cost. Its radiation tolerance for 10 years´ operation in the ATLAS cavern can be achieved as several pre-selection irradiation tests have shown. Before going to production this must be verified on larger samples. The implementation of the supervisory control system in PVSS has started. The basic elements are defined. Future test beam activities will allow us to test and improve the proposed control structure.

VII. References

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[6] www.atlas.uni-wuppertal.de/dcs

[14] from ETM, A-7000 Eisenstadt, Austria