Sorting Devices for the CSC Muon Trigger System at CMS

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Abstract

The electronics system of the Cathode Strip Chamber (CSC) muon detector at the CMS experiment needs to acquire precise muon position and timing information and generate muon trigger primitives for the Level-1 trigger system. CSC trigger primitives (called Local Charged Tracks, LCT) are formed by anode (ALCT) and cathode (CLCT) cards [1]. ALCT cards are mounted on chambers, while CLCT cards are combined with the Trigger Motherboards (TMB) that perform a time coincidence of ALCT and CLCT. Every combined CLCT/TMB card (one per chamber) transmits two best combined muon tags to the Muon Port Card (MPC) which serves one CSC sector (8 or 9 chambers). The MPC selects the three best muons out of 18 possible and sends them over 100 m of optical cable to the Track Finder (TF) crate residing in the underground counting room In the current electronics layout the TF crate has 12 Sector Processors (SP), each of which receives the optical streams from several MPC. The SP measures the transverse momentum, pseudo-rapidity and azimuthal angle of each muon and sends its data (up to 3 muons each) to the CSC Muon Sorter (MS) that resides in the middle of the TF crate. The MS selects the four best muons out of 36 possible and transmits them to Global Muon Trigger (GMT) crate for further processing.

Data sorting is the primary task of two devices in the CSC trigger chain: the MPC ("3 best muons out of 18") and MS ("4 best muons out of 36"). The total data reduction factor is 54. We propose a common approach to implementation of sorting logic and board construction for both the MPC and MS. They will be based on a single chip programmable logic devices that receive data from the previous trigger level, sort it and transmit the sorting result to the next trigger level. Programmable chips will incorporate input and output FIFO buffers that would represent all possible inputs and outputs for testing and debugging purposes. Finally we will use a common sorting scheme [2] for both designs. The MPC and MS functionality as well as the first results of logic simulation and latency estimates are presented.

I. Muon Port Card

In each of stations 2-4 of the CSC detector, an MPC receives trigger primitives from nine chambers corresponding to 60 degree sectors. Each MPC in these regions reduces the number of LCTs to three and sends them to the TF crate over optical cables. In station 1, an MPC receives signals from eight chambers corresponding to 20 degree sector. For these regions the number of selected LCTs is two. So the main sorting algorithm for an MPC is "3 best objects out of 18" while a "2 best objects out of 16" algorithm can be easily implemented as a subset of the main one.

Muon Port Cards will reside in the middle of 21-slot 9U*400 mm VME crates located on the periphery of the return yoke of the CMS detector. Other slots in a crate will be occupied by the TMB boards (9 or 8 total), DAQ Motherboards (9 or 8 total), Clock and Control Board and VME Master. The CCB is the main interface to CMS Trigger, Timing and Control (TTC) system. The VME Master performs the overall crate monitoring and control. All trigger/DAQ modules in a crate will communicate with each other over a custom backplane residing below a VME P1 backplane. Every bunch crossing (25 ns) an MPC will receive data from up to 9 TMB's, each of which is sending up to two LCT patterns. In the present design each LCT pattern is comprised of 32 bits (see Table 1). Data transmission from the TMB to the MPC at 80MHz would allow us to reduce the number of physical lines between the MPC and nine TMB's down to 288 and build a 6U backplane using industry standard 2 mm connectors. The MPC block diagram is shown on Figure 1. It performs a synchronization of incoming patterns with the local master

clock, sorting "3 out of 18" and output multiplexing of the selected patterns. The three best patterns are transmitted at 80Mhz to three 16-bit serializers that perform a parallel-to-serial data conversion with 8B/10B decoding for further transmission over optical cables to SP. The proposed serializer is a Texas Instrument TLK2501, and proposed optical module is a small form factor Finisar FTRJ-9519-1-2.5 transceiver [3].

The block diagram of the PLD is shown on Figure 2. Sorting is based on a 4-bit pattern which is a subset of the 9-bit quality code (Table 1). All 256-word deep FIFO buffers are available for read and write operations from VME. Data representing all input muons can be loaded into the input FIFO and sent out of FIFO at 80Mhz upon a specific VME command. The selected patterns will be stored in the output FIFO and transmitted to SP. Patterns coming from the TMB can also be stored in an output FIFO. This feature will allow us to test the MPC functionality and its communications with the TMB and SP without having the rest of trigger chain hardware.

Table 1: MPC Inputs and Outputs

Signal	Bits per input muon	Bits per output muon
Valid Pattern Flag	1	1
Quality	9	9
Cathode ½-strip ID	8	8
Anode Wire-Group ID	7	7
Accelerator Muon	1	1
Bunch Crossing ID	2	2
Reserved	4	-
CSC ID	-	4
Total	32	32

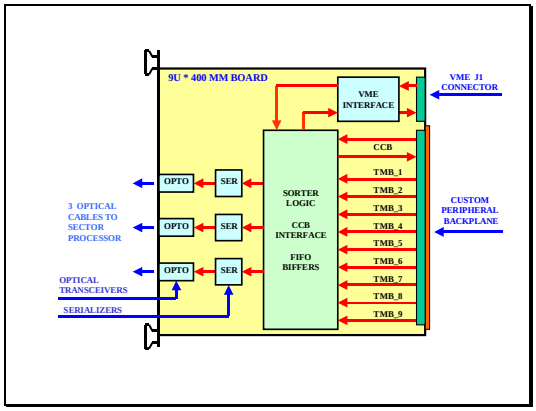

Figure 1: MPC Block Diagram

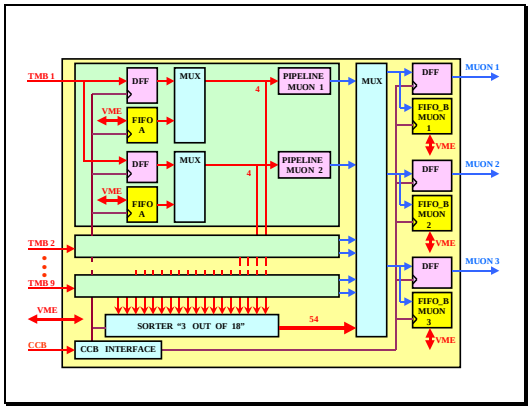

Figure 2: MPC Sorter PLD Block Diagram

II. Muon Sorter

Twelve SP's and one MS will reside in a single VME 9U*400 mm crate in the underground counting room. In addition to these modules there will be a Clock and Control Board (CCB) similar to a peripheral CCB, and a VME Master. Every bunch crossing an MS will receive data from 12 SP's, each of which is sending up to three patterns. Data transmission at 80MHz from the Sector Processors to the MS is envisaged; this would allow us to reduce the number of physical lines between MS and 12 SP's down to 360 and build a custom backplane using industry standard 5-row 2 mm connectors. Four such a 125-pin connectors are needed on a MS station in the middle of the custom 6U backplane residing below standard VME backplane.

The MS block diagram is shown on Figure 3. Its inputs and outputs listed in Table 2 are described in more details in [4]. Sorting is based on a 7-bit rank which represents the quality of each muon. The larger the rank, the better the muon for the sorting purpose. The MS performs synchronization of the incoming patterns with the local master clock, sorting "4 out of 36" and output multiplexing of the selected four patterns.

In addition to that, the MS performs a partial output LUT conversion to comply with the GMT input data format [5]. Parallel data transmission from the MS to the GMT at 40Mhz using LVDS drivers/receivers and separate cables for each muon was proposed by the GMT group. The Muon Sorter also utilizes the same idea used in the MPC of 256-word deep input and output FIFO buffers for testing purposes. The list of input and output signals is given in Table 2. A block diagram of the Muon Sorter main PLD is shown on Figure 4.

Table 2: Muon Sorter Inputs and Outputs

Inputs from Sector Processor			Outputs to Global Muon Trigger		
Signal	Bits per one muon	Bits per three muons	Signal	Bits per one muon	Bits per four muons
Valid Pattern Flag	1	3	Valid Pattern Flag	1	4
Phi Coordinate	5	15	Phi Coordinate	8	32
Muon Sign	1	3	Muon Sign	1	4
Eta Coordinate	5	15	Eta Coordinate	6	24
Rank	7	21	Quality	3	12
Bunch Crossing ID	-	2	Pt Momentum	5	20
Error	-	1	Bunch Crossing ID	4	16
			Error	1	4
			Clock	1	4
			Reserved	2	8
Total	19	60	Total	32	128

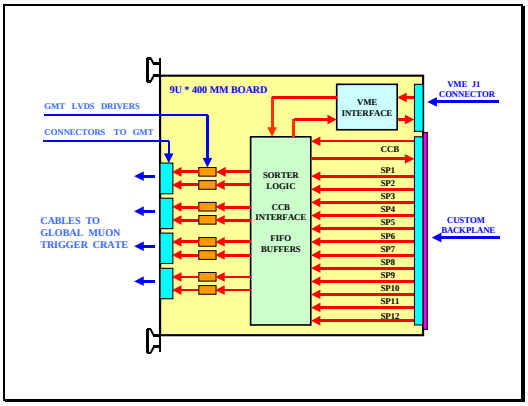

Figure 3: Muon Sorter Block Diagram

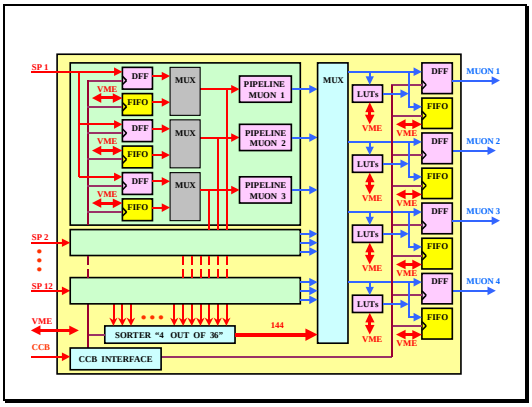

Figure 4: Muon Sorter PLD Block Diagram

III. Results of Simulation

PLD designs are implemented for the Altera 20KC family of PLD [6] using Quartus II ver. 1.0 design software. Preliminary results of logic simulation are shown in Table 3. They are obtained for the fastest available devices (-7 speed grade). We assume that the actual PLD latency means the time interval between the latching of the input patterns into the sorter chip at 80MHz and the moment when the selected best patterns are available for latching into the external device outside the sorter chip. Board latency for the MPC includes a delay for the output serialization. Particularly, for the TLK 2501 serializer this delay varies between 34 and 38 bit times, or 20..24 ns. For both devices an extra board delay of ~15ns is assumed. It includes the delay of the custom backplane receivers, signal propagation times and the delay of output LVDS drivers (for MS only).

Table 3: Results of Simulation

	Muon Port Card	Muon Sorter
Number of data inputs	288 @ 80 Mhz	384 @ 80 Mhz
Number of data outputs	48 @ 80 Mhz	128 @ 40 Mhz
Number of bits used for sorting	4	7
Altera PLD Device	EP20K400CF672C7	EP20K1000CF33-7
Number of logic cells (LC) used	9637/16640 (57%)	22716/38400 (59%)
Number of ESB bits used	184320/212992 (86%)	262144/327680 (80%)
Actual PLD latency, nanoseconds	75	150
Board latency, nanoseconds	115	165

IV. Conclusion

We have proposed a common approach to design and implementation of two sorting devices for the CSC Muon Trigger system. These designs are targeted tosingle programmable chips for both Muon Port Card and Muon Sorter. Results of preliminary simulation for the fastest Altera PLD indicate a maximum board latency of 115 ns for the Muon Port Card and 165 ns for the Muon Sorter. The MPC and MS prototypes are planned to be built in 2002 and 2003 respectively.

V. References

[1]. J. Hauser. Primitives for the CMS Cathode Strip Muon Trigger. Proceedings of the Fifth Workshop on Electronics for LHC Experiments. Snowmass, Colorado September 20-24, 1999. CERN/LHCC/99-33. Available at: http://hep.physics.wisc.edu/LEB99/

[2]. M.Matveev. Implementation of the Sorting Schemes in a Programmable Logic. Proceedings of the Sixth Workshop on Electronics for LHC Experiments. Krakow, Poland 11-15 September 2000. Available at: http://lebwshop.home.cern.ch/lebwshop/LEB00_Book/posters/matveev1.pdf

[3]. M.Matveev, T.Nussbaum, P.Padley. Optical Link Evaluation for the CSC Muon Trigger at CMS. These proceedings.

[4].The CMS TriDAS Project Technical Design Report, Volume 1: The Trigger System. Chapter 12. Available at: http://cmsdoc.cern.ch/cms/TDR/TRIGGER-public/CMSTrigTDR.pdf

[5]. Proposal for a common data link from the RPC, DT, CSC Regional Muon triggers to the Global Muon Trigger vers.3a. Available at: http://wwwhephy.oeaw.ac.at/p3w/cms/trigger/globalTrigger/Hardw/Interfaces/Input/Reg_to_GT_Muon3.pdf

[6].http://www.altera.com/products/devices/apex/apx-index.html